SST Camera:
Design Report

SST Camera Project Document No.

SST-CAM-DSR-001

Version

2.a

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Table of Contents

1 Introduction

1.1 Scope & Purpose of this document

The purpose of this document is to summarise the design of the SST Camera, including architecture and technical implementation.

1.2 Context

SST Cherenkov Cameras will be provided as part of the SST in-kind contribution to the CTA Observatory. The SST Camera design iteration started following approval of the SST Programme Proposal [RD1] by the CTAO Council. The SST Programme encompasses the SST Structure Project (SST-STR), the SST Camera Project (SST Camera).

Following the recommendation of the CTAO Council [RD2], the design of the SST should be based on the ASTRI/CHEC prototypes, incorporating experience gained from all designs. The design of the SST Camera presented here is then an evolution of the Compact High Energy Camera (CHEC) design, in its SiPM-based variant (CHEC-S) [RD3].

1.3 Applicable Documents

[AD1] SST Camera Prototype Lessons Learnt (SSTER-CAM03-PDR-PLL) (link)

[AD2] SST Camera: Engineering Development & Verification Plan (SST-CAM-PLA-009)

[AD3] SST Camera: Subsystem Technical Requirements Specification (SST-CAM-SPE-002)

[AD4] SST Programme: Telescope Architecture and Design-Summary Report (SST-PRO-DSR-002)

[AD5] SST Programme: STR-CAM Interface Control Document (SST-PRO-ICD-007)

[AD6] SST Programme: Telescope Concept of Operations (SST-PRO-OPD-001)

1.4 Reference Documents

[RD1] SST Programme Proposal (link)

[RD2] CTAO Council Resolution regarding the SST harmonization C17-19

[RD3] Commissioning and Performance of CHEC-S – a compact high-energy camera for the Cherenkov Telescope Array, J.J Watson and J. Zorn, 2019 (link)

[RD4] SST Camera Prototype Design Report (SSTER-CAM03-PDR) (link)

[RD5] HPK SST Camera SiPM Data Sheet (link)

[RD6] SST Camera Internal Report: SiPM Selection (to be released)

[RD7] SST Camera Internal Report: Focal Plane Electronics R&D (to be released)

[RD8] SST Camera Internal Report: Focal Plane & Electronics Thermal Analysis (link)

[RD9] TARGET5: Anewmulti-channeldigitizerwithtriggeringcapabilitiesforgamma-rayatmospheric Cherenkov telescopes, Funk et al., 2016 (link)

[RD10] SST Camera Production Plan (SSTER-CAM06-PP) (link)

[RD11] SST Programme: On-site AIT Plan (SST-PRO-PLA-012)

[RD12] CTA Interface Control Document for ACADA – Generic Telescope Control, Doc. No. CTA-ICD-SEI-000000-0002, Issue 2, Rev.: h, 30.4.2020 (link)

[RD13] CTA Telescope State Machine, Doc. No. CTA-SPE-ACD-000000-0001, Issue 2, Rev e, 17.3.2020 (link)

[RD14] Muon tagging on the Backend-Electronics of CHEC-S -- a compact high-energy camera for the Cherenkov Telescope Array, Pillera et al., 2019 (link)

1.5 Definition of Terms and Abbreviations

ASL	Above Sea Level
AC	Alternate Current
ACADA	Array Control and Data Acquisition
ADC	Analogue to Digital Converter
AIT	Assembly, Integration, Testing
API	Application Programming Interface
ASIC	Application Specific Integrated Circuit
ASTRI	Astrophysics with Italian Replicating Technology Mirrors
AXI	Advanced eXtensible Interface
BEE	Back-End Electronics
BP	Backplane
CAD	Computer Aided Design
CBE	Current Best Estimate
CHA	Chiller Assembly
CHEC	Compact High Energy Camera
CHEC-S	A CHEC prototype camera for the SST based on SiPMs
CMT	Camera Maintenance Tools
COTS	Commercial Off-The-Shelf
CSS	Camera Support Systems
CSW	Camera Control Software
CTA	Cherenkov Telescope Array
CTAO	Cherenkov Telescope Array Observatory
CU	Camera Unit
DC	Direct Current
DCR	Dark Count Rate
DESY	Deutsches Elektronen-Synchrotron
DIN	Deutsches Institut für Normung
DOC	Documentation
DSO	Digital Oscilloscope
DVER	Design Value Engineering Review
EIA	External Illumination Assembly
EM	Electromagnetic

ENC	Enclosure
ERA	Electronics Rack Assembly
ESD	Electrostatic Discharge
EXC	External Cabling
FEE	Front-End Electronics
FEM	Finite Element Method
FET	Field-Effect Transistor
FLA	Flasher Assembly
FoV	Field of View
FPA	Focal Plane Assembly
FPE	Focal Plane Electronics (Assembly)
FPGA	Field Programable Gate Array
FPM	Focal Plane Mechanical (Assembly)
FPP	Focal Plane Plate
FW	Firmware
FWHM	Full Width Half Maximum
Gbps (Gb/s)	Gigabit per second
GECCO	Generic Ethernet-Chainable COntrol
HPK	Hamamatsu Photonics K.K.
HV	High Voltage
I/O	Input / Output
I^2C	Inter-Integrated Circuit
IC	Integrated Circuit
ID	Identification
L1	Level 1 (trigger)
L2	Level 2 (trigger)
LED	Light Emitting Diode
LIDAR	LIght Detection And Ranging
LL	Lesson Learnt
LVDS	Low Voltage Differential Signal
M1	SST Primary Reflector
M2	SST Secondary Reflector
MC	Monte Carlo (simulation)
MC	Monte Carlo
MEV	Maximum Expected Value
MPIK	Max-Planck-Institut für Kernphysik
MST	Medium Sized Telescope
MTP/MTO	Multifiber Termination Push-on/Pull-off
NSB	Night Sky Background
OCT	Optical Cross-Talk
PBS	Product Breakdown Structure
PCA	Printed Circuit Assembly (i.e., populated PCB)
PCB	Printed Circuit Board

PDE	Photon Detection Efficiency
pe	Photoelectron(s)
PID	Proportional-integral-derivative
PM	Project Manager
PMMA	Polymethyl Methacrylate
PPS	Pulse Per Second
PPSA	Power Panel Subassembly
PSF	Point Spread Function
PSU	Power Supply Unit
PSU	Power Supply Unit
PWM	Pulse Width Modulation
QBP	Quarter Backplane
RH	Relative Humidity
RMS	Root Mean Square
RPC	Remote Procedure Call
RPM	Revolutions per Minute
S/C	Slow Control
SB	Slow Board
SCA	Slow Control Assembly
SE	Systems Engineer
SFP	Small Form-factor Pluggable
SiPM	Silicon Photomultiplier
SP	Superpixel
SPI	Serial Peripheral Interface
SST	Small Sized Telescope
SW	Software
SWAT	Software Array Trigger
SWF	Software and Firmware
TARGET	TeV Array Readout with GSa/s sampling and Event Trigger
TB	Timing Board
TBC	To be confirmed
TBD	To be determined
TCP	Transmission Control Protocol
TDC	To be confirmed
TM	TARGET Module
UDP	User Datagram Protocol
UV	Ultraviolet
WBS	Work Breakdown Structure
WR	White Rabbit

2 Design Summary

The SST Camera forms the detector element of the CTA Small-Sized Telescopes (SSTs). The SSTs offer an opportunity to provide CTA with unprecedented sensitivity and the highest angular resolution of any instrument operating above X-rays. To achieve this many SSTs are required. An optimal SST camera is therefore low-cost, reliable and easily maintainable. Such a camera should have a large FoV (to capture large and off-axis images), have fine pixelization (to resolve small images and isolate signal from background) and have a large readout window (to fully contain images with a large time gradient).

Figure 1 shows an overview of the SST Camera, which contains 2048 pixels instrumented by 32 tiles each containing 64 SiPM 6×6 mm^2 pixels, proving an ~9° FoV. Tiles are arranged in the focal plane to approximate the radius of curvature resulting from the telescope optics. Each tile is connected to a set of Focal Plane Electronics (FPE) and a TARGET Module (TM); to provide SiPM control and monitoring, pulse-shaping & amplification, digitisation at 1 GSa/s (using TARGET CTC ASICs) and the first level of triggering (using TARGET CT5TEA ASICs). All TMs are connected to a single backplane (BP) that provides the camera-level trigger and a 10 Gbps connection for data. An array-wide White Rabbit system connected inside the camera provides absolute timing. The camera can operate in the presence of significant NSB, and readout events at up to 1200 Hz. The camera includes an illumination system to provide calibration via fast, variable intensity, flashes. A flat, glass, entrance window and external door system provide protection from the elements. Thermal control is via an external chiller. Fans internal to the camera circulate the resulting cooled air. The camera is hermetically sealed and a breather-desiccator maintains an acceptable level of humidity. Figure 2 shows an overview of the core camera functionality.

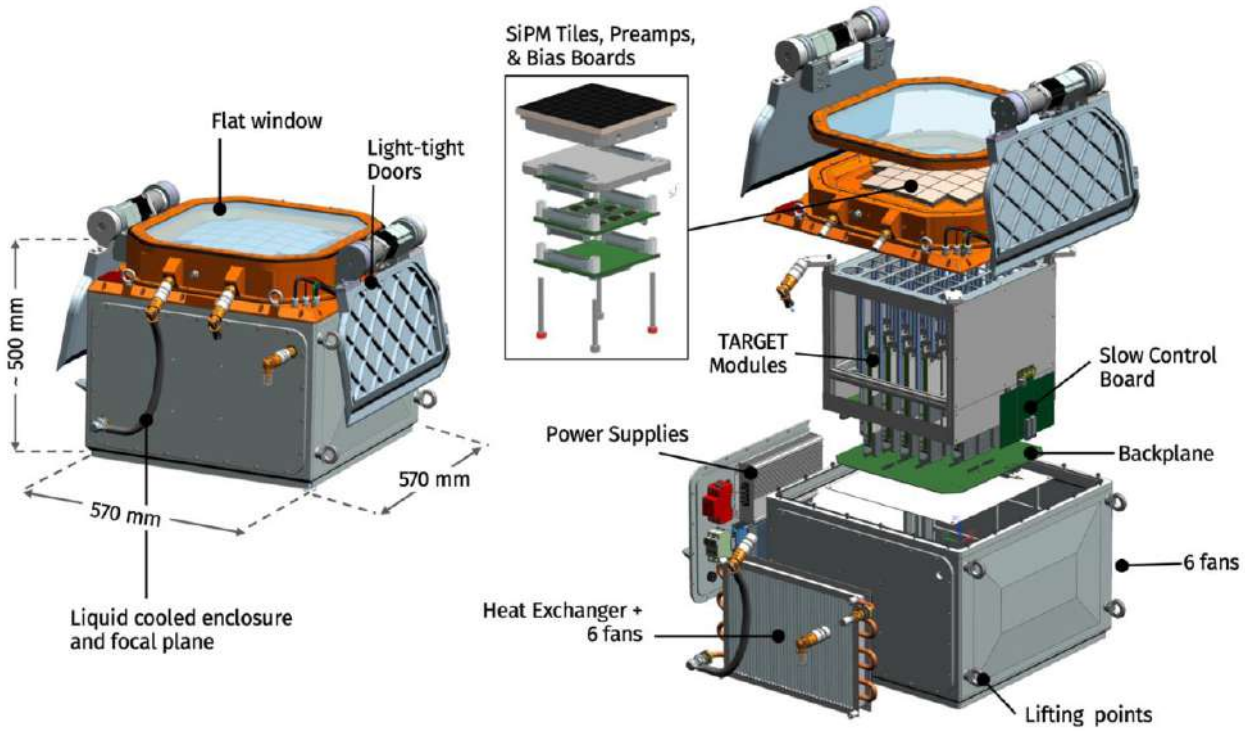


Figure 1: SST Camera CAD overview

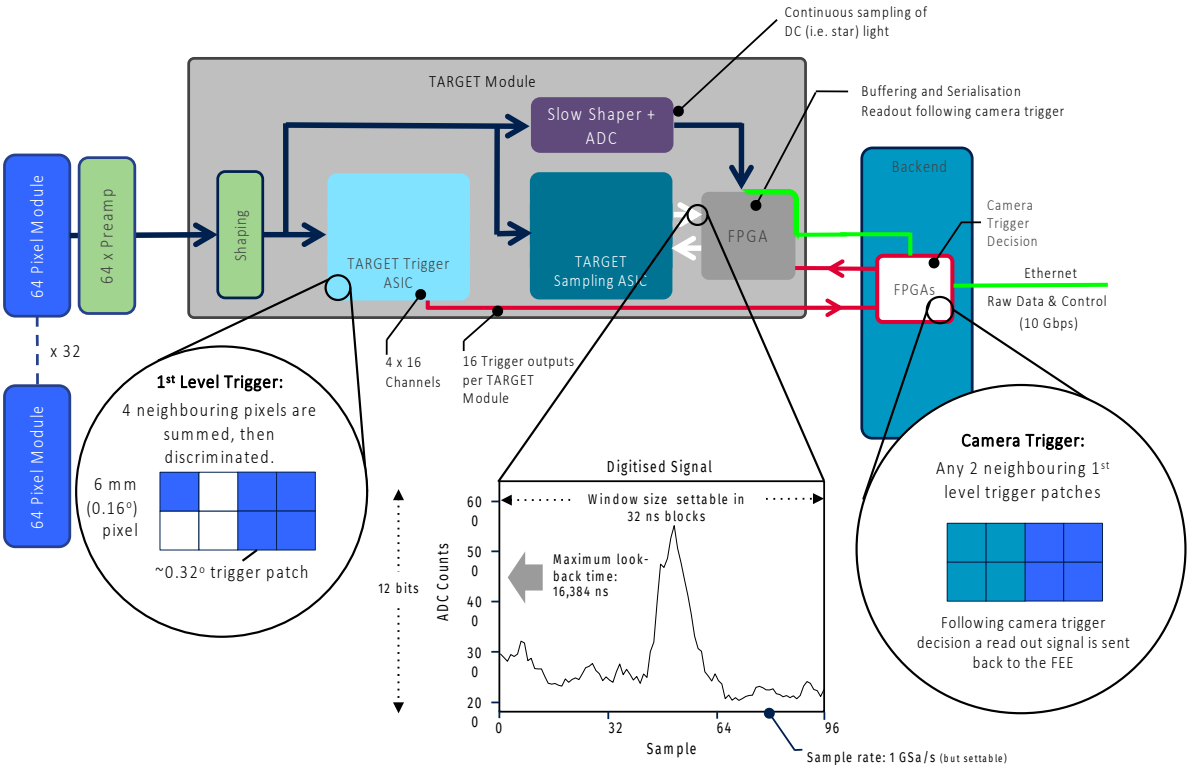


Figure 2: SST Camera core functionality.

3 Product Breakdown Structure

The high-level camera Product Breakdown Structure (PBS) is shown in Figure 3 and explained below.

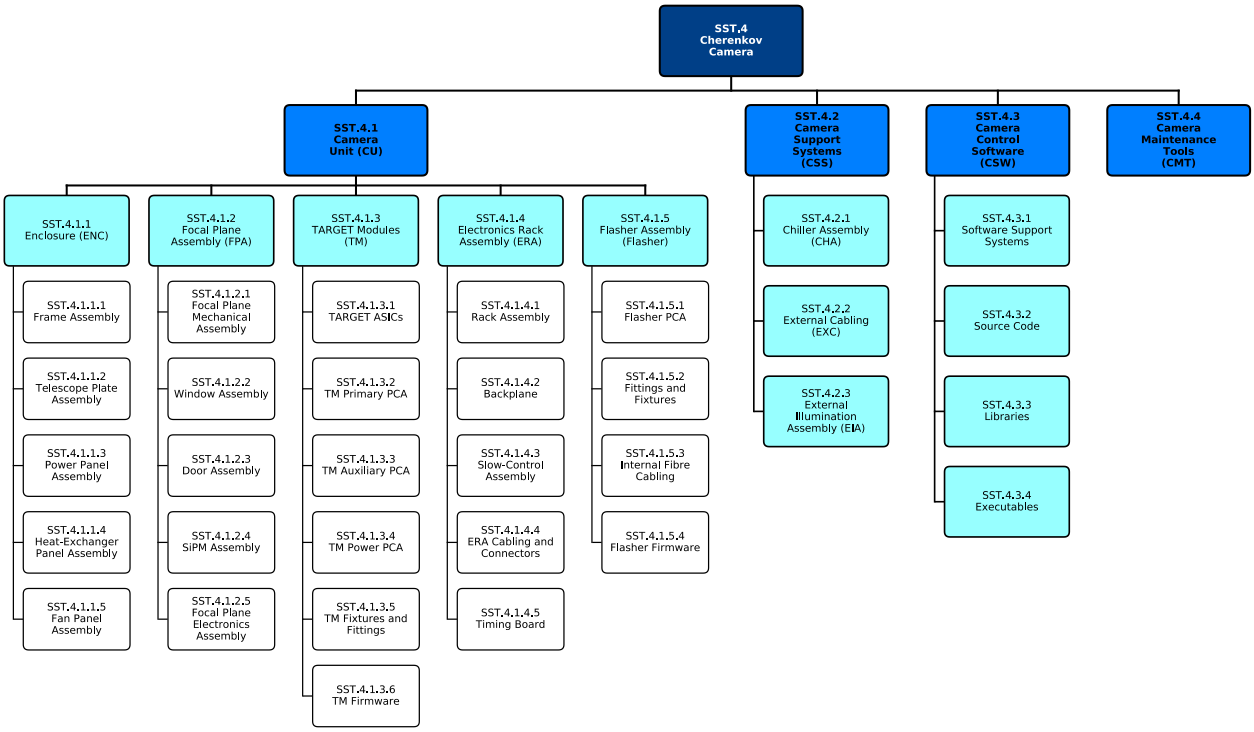


Figure 3: SST Camera Product Breakdown Structure

- **Camera Unit (CU)**: The physical camera, as mounted in the focal plane of the SST.
    - **Enclosure (ENC):** The camera case, including thermal exchange system and power supply system. The enclosure measures approximately 57 cm x 57 cm x 45 cm and is made from machined Al. components. The ENC accepts an AC 220 V input connection for power, a multi-core fibre connection for data and control and refrigerant fluid inlet and outlet.
    - **Focal Plane Assembly (FPA):** SiPMs are mounted on a liquid-cooled plate providing temperature stabilisation. A coated entrance window protects the SiPMs. A motorised door protects the camera when not in use. Preamplifiers, bias-voltage supply boards and interface boards form the Focal Plane Electronics (FPE), connected to the SiPMs. The FPA also houses a scintillating fibre for SiPM calibration, running in a loop at the underside of the window and connected inside the camera to an LED flasher unit.
    - **TARGET Modules (TM):** The 32 TARGET Modules, providing the first level of triggering and the digitisation of signals from the FPA.
    - **Electronics Rack Assembly (ERA):** The rack that the TM are slotted into, housing a Backplane for camera-level triggering and read out, Timing Board for precision time stamps, and SCA

(Slow-Control Assembly) for control of the camera doors, the camera power distribution and monitoring of the environment inside the camera.

  - Flasher Assembly (FLA): The LED Flasher-based calibration system. Installed in the CU, with connection Flasher to scintillating fibre (part of the FPA), to a diffuser for illuminating M2 and to a fibre connected to a diffuser at M2 (part of the CSS).

- Camera Support Systems (CSS): Field elements needed to support the CU on/at the SST.

  - Chiller Assembly (CHA): The camera chiller and associated pipe work.

  - External Cabling (EXC): All cabling external to the CU and attached to the CU and routed via the Telescope Structure.

  - External Illumination Assembly (EIA): The external illumination fibre, routed to M2 and coupled to an optical system to illuminate the camera.

- Camera Control Software (CSW): Any and all SW needed for the control, readout, and monitoring of the CU & CSS, installed on the CTAO computing farm. It should be noted that no SW is installed in the CU. A physical camera server is provided by CTAO Computing and CSW is installed there.

- Camera Maintenance Tools (CMT): Any and all items needed onsite by CTAO to access and maintain the CU, CSS, CSW, not provided by CTAO. This item is to be further broken down, but includes the Camera transport / storage container, spare subsystem / part transport and storage containers, the on-site workshop camera maintenance setup and tools, the on-site camera-to-structure mounting tools (e.g., lifting harness).

4 Camera Architecture

This section presents the architectural design of SST Camera, flowing down from the overall SST architecture ([AD4]) and describes the logical relationship between subsystems and the flow of commands, signals and data. The section is broken down as:

- Data Capture & Readout
- Triggering
- Time Synchronisation
- Control & Monitoring
- Power, Thermal and Environmental Control

In the schematic figures included in this section, the colour-coded boxes represent second-level PBS items corresponding to actual devices or subassemblies, arranged in a way that suggests their physical placement in the camera.

A schematic view of the overall SST Camera architecture is shown in Figure 4. In it, the top-level PBS groups are colour coded, and their names are mostly self-explanatory.

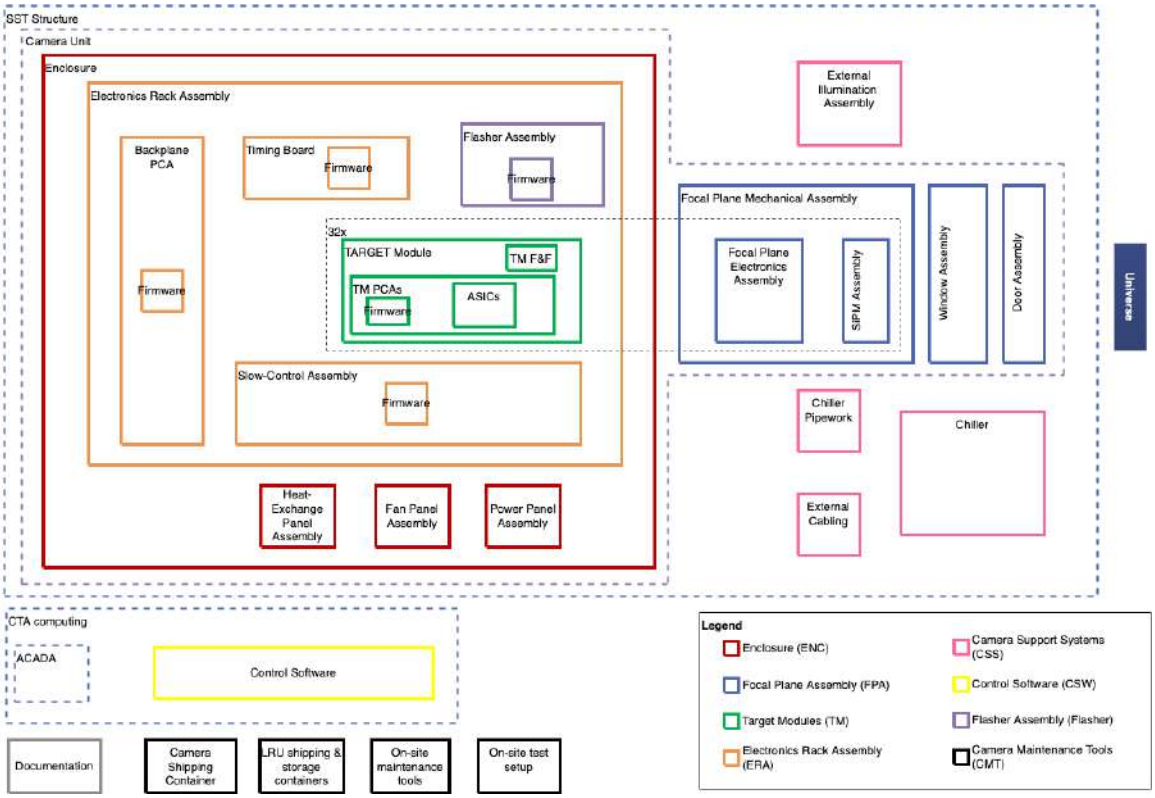


Figure 4: Schematic view of the SST Camera architecture

4.1 Data Capture and Readout

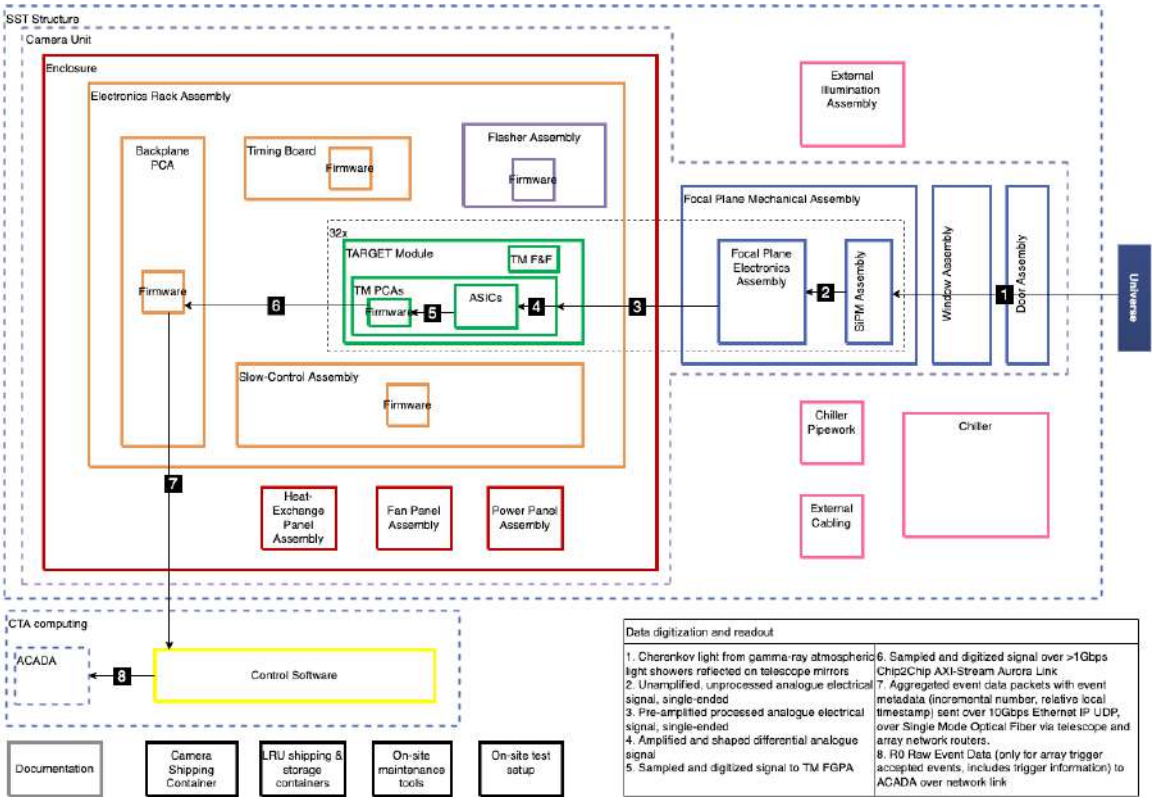


Figure 5: Schematic view of the data digitisation and readout architecture

The SST Camera digitisation and readout architecture is illustrated schematically in Figure 5. Following steps 1 – 8 from the right to the left of the diagram:

(1) Cherenkov and background light from the NSB are focused by the SST Telescope mirrors onto the camera. If the Door Assembly is open, the light passes through the Entrance Window and reaches the surface of the SiPM Assemblies, part of the Focal Plane Assembly.

(2) Some fraction of incident photons is converted to electrical signals by the SiPMs. These signals then reach the Pre-amplifier Assembly inside the Focal Plane Electronics.

(3) The Pre-amplifier Assembly hosts low-noise amplifiers that amplify the signal and send it over coaxial cables to the TARGET Module, via interface PCBs.

(4) On the TARGET Module, the signal is further amplified, split into three branches and shaped. One signal branch is sent to the sampling TARGET ASICs, which continuously store it in an analogue ring-buffer memory implemented with a switched capacitor array. A second one is used for triggering, and a third one is used for the slow signal (see Section 4.6 in [RD4]).

(5) Upon arrival of a data readout request from the Backplane (see Section 4.2), the signal waveform in the time window of interest is digitised by the TARGET ASIC. The waveform data is then read out by the TM FPGA firmware, which sends it to one of the Backplane FPGAs (6).

(7) The Backplane aggregates all data belonging to the same event, adds some additional information such as the incremental event number and the relative local timestamp, and sends it to the Event Builder software running on the Camera Server over 10Gbps Ethernet.

(8) The Event Builder software process collects the event data and the event absolute timestamps coming from the timing system (see Section 4.3), merges and buffers them. In case an event is requested by the CTA array trigger, the Event Builder sends its data in an agreed-upon format to the CTA ACADA system for further reduction and storage.

4.2 Triggering

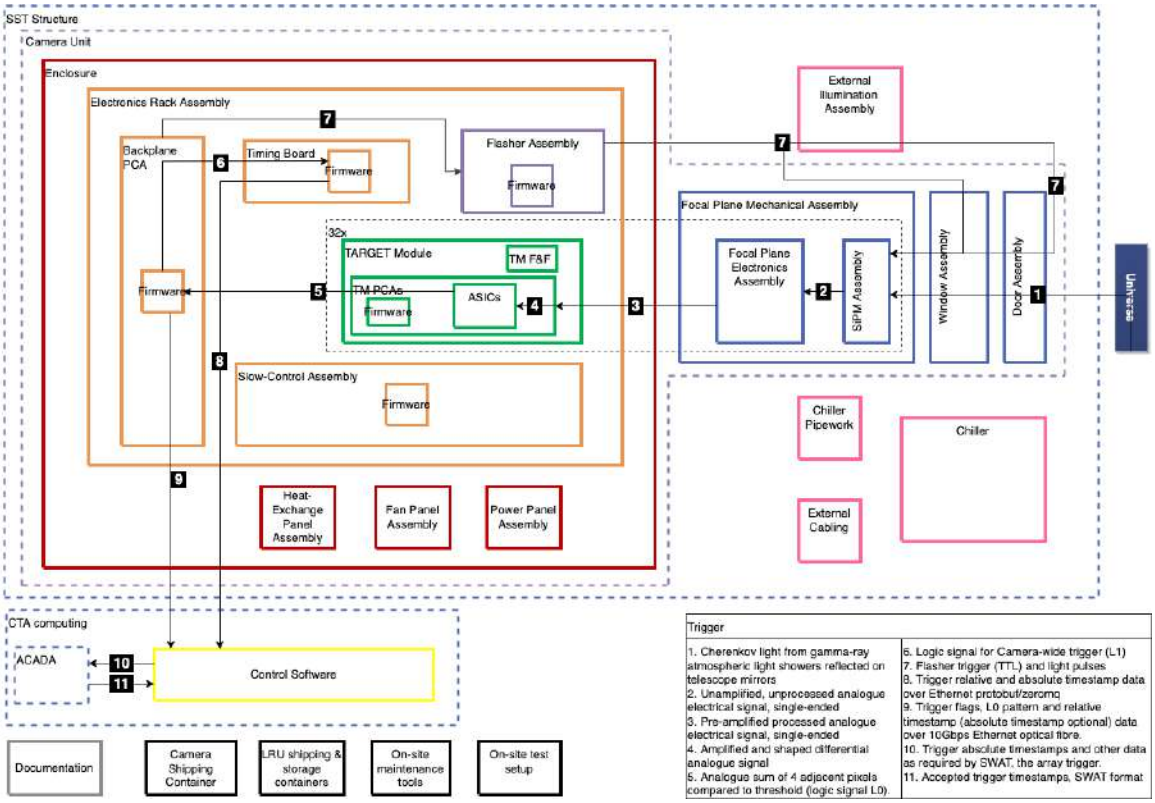


Figure 6: Schematic view of the trigger architecture

The SST Camera trigger architecture is illustrated schematically in Figure 6. Steps (1) (2) and (3) are exactly the same as the data architecture described in Section 4.1.

(4) A signal branch from the amplification electronics of the TARGET Module is routed to the triggering TARGET ASICs. These ASICs compare the analogue sum of the signals of groups of four adjacent pixels to a configurable threshold value. The groups of four pixels are called super-pixels, and the output of this operation is a logic signal called the L0 trigger signal.

(5) This signal is stretched and routed directly to the backplane FPGAs. There, backplane firmware evaluates the coincidences of any two neighbouring L0 signals across the camera. When such a coincidence is found, an L1 (camera-level) trigger signal is generated. The trigger causes the data stored in the TARGET chip analogue memories to be read out, and some trigger metadata such as the local relative timestamp and the event number to be appended to it, as explained in Section 4.1.

(6) When an L1 trigger happens, a signal with fixed latency is sent to the timing board, for absolute timestamping.

(7) An L1 trigger signal can also be generated by the backplane in sync with the trigger pulse sent to the Flasher; which then generates a light flash that illuminates the camera for calibration purposes. This happens during dedicated calibration runs and during normal observation runs, interleaved with the camera triggers from Cherenkov showers. The backplane can also generate a L1 trigger from an internal periodic trigger generator (so-called pedestal triggers), or from a remote software request.

(8) The timing board upon receiving an L1 trigger sends the relative and absolute timestamps of the event to the Camera Server over an Ethernet link.

(9) The logical state of the L0 trigger signals at the trigger time, together with a complete set of trigger data, including the trigger source and the relative timestamp and event number, is sent to the Event Builder software running on the Camera Server over a 10Gbps Ethernet link.
(10) The Event Builder is interfaced to the Software Array Trigger (SWAT) subsystem, which is part of the CTAO ACADA system. Upon receiving (8) and (9), the Event Builder buffers event timestamp information, and sends to the SWAT after appending additional information as required by the interface definition.
(11) The SWAT replies with information on which events are accepted for transmission. Only then, the Event Builder sends the accepted events data to ACADA (step 8 in Section 4.1).

4.3 Time Synchronisation

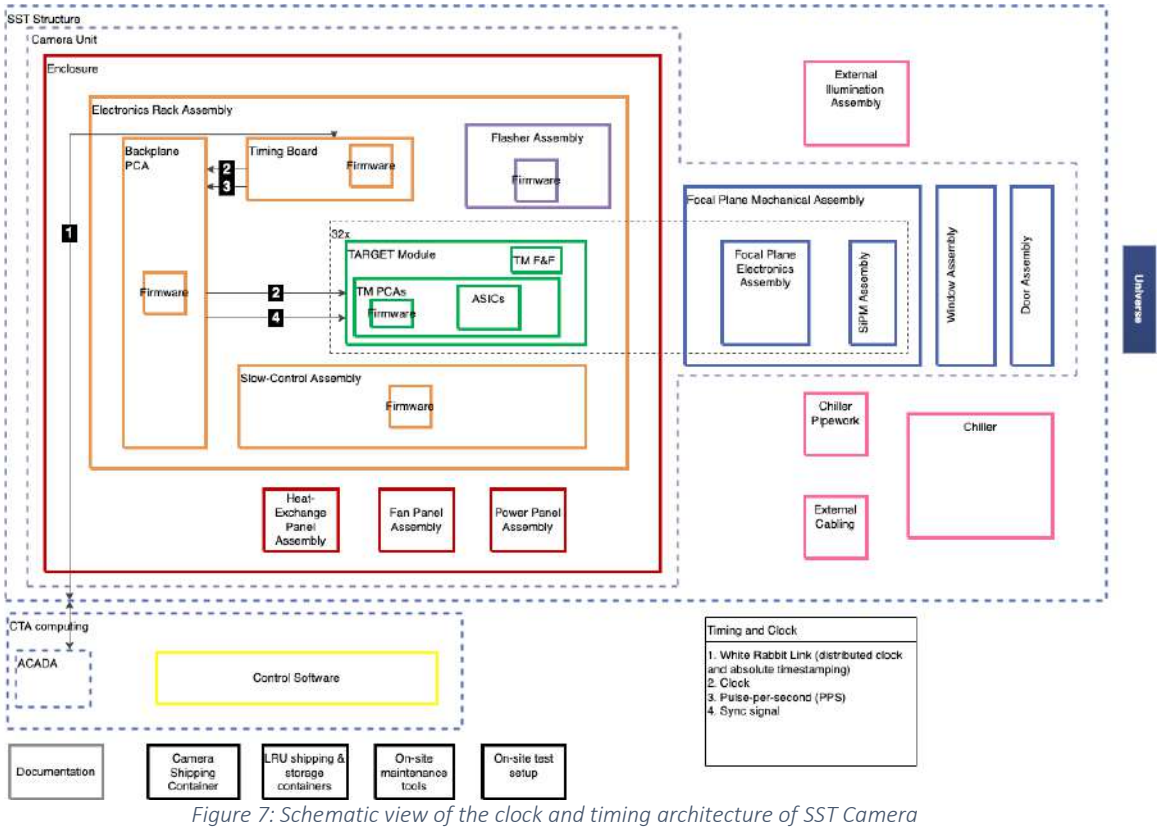


Figure 7: Schematic view of the clock and timing architecture of SST Camera

The SST Camera clock and timing architecture is illustrated in Figure 7.

The Timing Board is a White Rabbit (WR) node in the CTAO timing network. The White Rabbit protocol allows for the distribution of clock and absolute time from a central location with sub-nanosecond precision, self-correcting for signal path delays (1).

The Timing Board sends two signals to the Backplane: a 125 MHz clock (2), and a Pulse Per Second (PPS) signal (3). It also receives trigger and busy signals from the backplane, for which it generates absolute timestamps for the use in sub-array-level trigger formation and event selection (see previous section). The backplane runs on the clock provided by the Timing Board, and in turn provides the clock and a synchronisation signal (4) to the TARGET Modules. This establishes a synchronized time reference shared by Backplane and TARGET Modules.

Using this time reference, both Backplane and TARGET Modules can assign a timestamp to each event. This timestamp is relative to the sync epoch and not absolute as the one given by Timing Board. It is used for aggregating the TM event data into complete camera events. More importantly, it allows the Backplane to identify the time window of interest for the readout, and enables asynchronous, pipelined data readout requests to the TARGET Modules. This asynchronous readout capability reduces the deadtime of the camera to close to zero.

4.4 Control and Monitoring

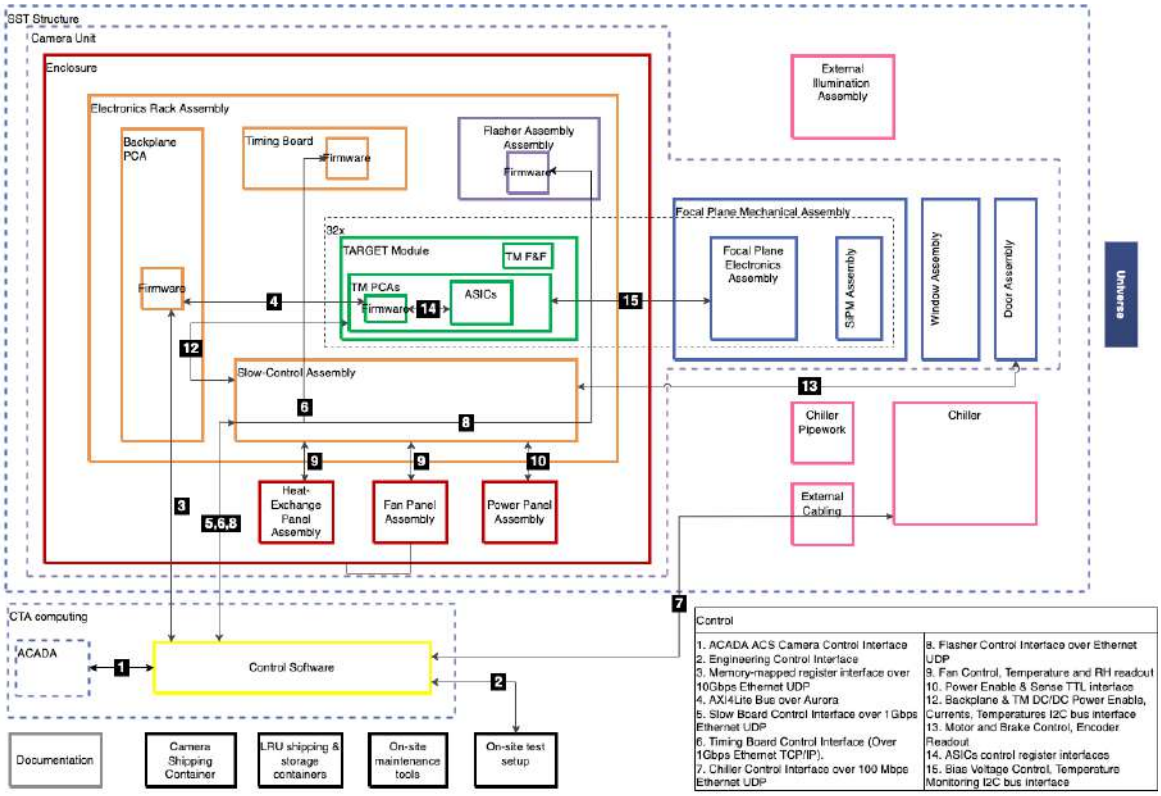


Figure 8: Schematic view of the control and monitoring architecture of SST Camera.

The SST Camera control and monitoring architecture is illustrated in Figure 8. In this figure, the primary source of control commands and the destination of monitoring, logging and housekeeping information is the CTAO ACADA system, which is connected via the on-site network to the Camera Controller software running on the Camera Server (1). This interface honours the specifications of the ACADA ACS Camera Control Interface.

The CSW then has internal RPC interfaces between a high-level manager to low-level hardware-control software, a collection of processes implementing low-level protocols to remotely control the actual camera hardware via the dedicated Ethernet link to the Camera. A lower-level source of control commands is the Engineering/Expert User Interfaces provided as part of the on-site test and monitoring tools (2)

The Backplane receives control commands as UDP packets over a 10 Gbps Ethernet link; these packets are interpreted as register interface (read or write) commands for the memory-mapped registers of both the Backplane and the TM modules firmware. There is an AXI4Lite bus interface between the Backplane and the TMs (4) that exposes the TM registers to the Backplane and

ultimately to the Camera Software. At lower level, the TARGET Module FPGAs control and monitor the TARGET ASICs via their custom control register interfaces (14), and control and monitor the bias voltage and temperature of the Focal Plane Electronics via I^2C bus (15).

The Slow Control Assembly also receives commands from the Camera Control Software via UDP packets over a 1 Gbps Ethernet interface (5). It also acts as an Ethernet router for control packets to the Timing Boards (6) and to the Flasher (6).
At a lower level, the Slow Control Assembly has the following functions:

- Control and monitoring of fan speed, temperature and humidity to the heat-exchanger and fan panels (9).
- Control of the Power Supply Units with simple sense/enable lines (10) and (11).
- Control of the main DC/DC converters on the Backplane and the TARGET Modules, and monitoring of their power consumption via I^2C bus (12).
- Control and monitoring of the Door motors and position sensors (13).

Finally, the Camera Control Software also controls the Chiller via UDP packets over a 100 Mbps Ethernet connection, via the Telescope internal Ethernet network.

4.5 Power, Thermal and Environmental Control

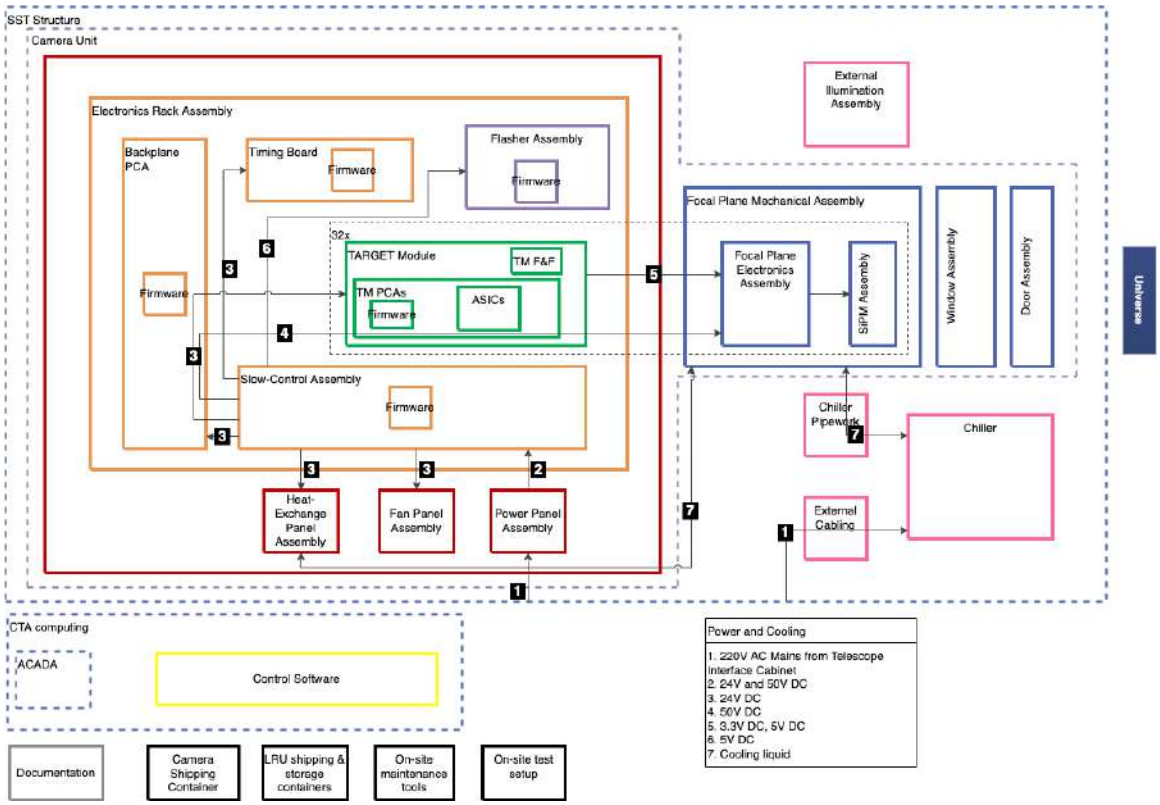


Figure 9: Schematic view of the Camera power supply and distribution and thermal/environmental control architecture

The Camera power supply and distribution, thermal and environmental control architecture is illustrated in Figure 9. The 220V AC Mains come via interfaces to the SST Telescope Structure (1), enter the Camera Unit through the Power Panel Assembly, where 24V and 48V DC are generated by the two Power Supply Units. The Chiller is also powered from 220 V.

There are two Power Supply Units, one for 24V and another for 48V. They are connected to the Slow-Control Assembly (2), which distributes the power as follows:

- 24V to the Backplane (3),
- 24V to the Timing Board (3)
- 24V to the TARGET Modules (3, through the Backplane)
- 48V to the Biasing Assembly in the Focal Plane Electronics (4, via the Backplane and the TARGET Modules),
- 24V to the two fan trays of the Heat-Exchanger Panel Assembly and Fan Panel Assembly (3).

The Slow Control Assembly also provides 5V to the Flasher Assembly (6).

The TARGET Modules provide the 5V, 3.3V required by the Pre-amplifier Assembly in the Focal Plane Electronics (5).

The cooling fluid (7) flows from the Chiller to the Focal Plane Plate, then to Heat-Exchanger Panel Assembly, and back to the Chiller.

5 Design History

The design of the SST Camera is an iteration of the CHEC-S prototype design [RD4]. Two CHEC prototypes have been built and tested. The first, CHEC-M, was based on multi-anode PMTs (MAPMs) and served as a proof of principle of the digitisation, trigger, control and readout systems. CHEC-M underwent extensive lab tests and was deployed on the GCT prototype structure in Meudon, where it was used to record the first Cherenkov images seen by a CTA prototype.

The second prototype camera, CHEC-S, was based on SiPMs (Figure 10). CHEC-S uses Hamamatsu S12642-1616PA-50 SiPMs. Each 6 x 6 mm^2 camera pixel was made up by combing four 3 x 3 mm^2 SiPM pixels. The FEE modules used in CHEC-S were based around the TARGET-C and TARGET-T5TEA ASICs. The CHEC-S back-end electronics consisted of a separate Backplane, XDACQ and Timing Board. The camera-level trigger and readout scheme fulfilled all requirements. The slow control system in CHEC-S was based on separate control and power boards, with a simple COTS µ-controller. The power distribution system used in CHEC-S consisted of external 12 V supplied via a bulky cable, leading to an external power supply. The CHEC-S entrance window, was curved to follow the camera focal plane, and made from uncoated PMMA. CHEC-S (without chiller) consumed ≈1 kW in power, weighed ≈50 kg and measured ≈50 cm x 50 cm x 50 cm (excluding protruding panels and open doors).

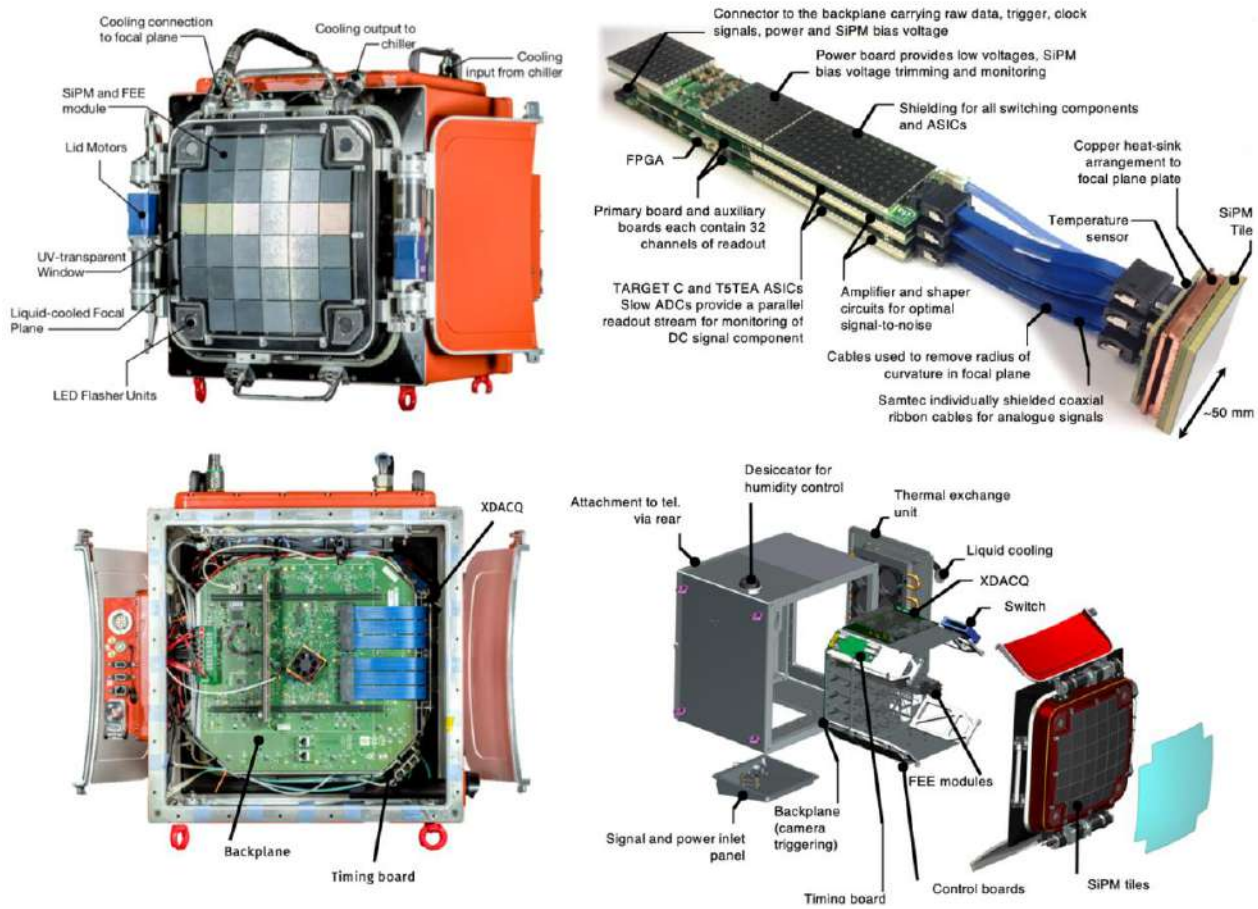


Figure 10: Overview of the CHEC-S prototype camera.

6 Development Strategy

All components of the SST Camera have been prototyped via CHEC-S. Changes were made to address lessons learned and improve reliability, maintainability and manufacturability. Changes were considered against the constraints of: cost, time, resources, and technological risk. The following guidelines/principles have been followed:

- Simplify camera architecture & assembly concept
  - Reduce number of devices, computing architectures and embedded systems
  - Minimize and optimize all internal interfaces
  - Minimize cables and connectors
- Increase commonality
  - Use common electronic designs for the camera sub-systems
  - Maximise commonality of components and schematics
  - Common software and firmware framework
- Use standard industry solutions where possible
  - Mechanical assembly
  - Cabling
  - Control protocols
  - Software design patterns

A summary of the design changes, including a reference to the applicable lessons-learnt [AD1] are given in Table 1. There are several changes requiring substantial effort.

The following items will be developed to verify the camera design:

- Testable Elements
  - Window Assembly
  - TARGET Modules (TM)
  - Camera Modules (CM) (Mini-window, SiPM tile, FPE, TM)
  - ¼ Backplane (QBP), then full BP
  - Chiller
  - Flasher
  - Slow-Control Assembly (SCA)
  - Door Bench Assembly
- Mechanical Camera (MCAM)
  - Window Assembly, Focal Plane Mechanics and Enclosure
- ¼ Camera (QCAM)
  - Full set of mechanics, working doors, SCA, and 8 of 32 SiPM tiles, FPE, and TMs connected to the QBP.
- Engineering Camera (ECAM)
  - First full Cherenkov camera.
- ECAM-On-Telescope
  - The Engineering Camera install on a prototype telescope structure.

For further information about the development path and status see [AD2].

The status of the technical development of each Camera subsystem is given in Section 0.

Table 1: Overview of the changes to the CHEC-S design. Refer to [AD1] for the Lessons Learnt (LL) codes. "Progress": 0% = not started, 20% = concept complete, 40% = R&D complete, 60% = design complete, 80% = full scale model ready, 100% = fully validated

	Planned Design Changes	Severity of Change	Progress	Reasoning / Lessons Addressed
Camera Unit				
ENC	Increase internal camera volume Include 220 V power supplies Include second set of fans Improve O-ring retention	Medium	70%	LL32, LL33, LL37, LL41 LL45 LL30, LL31, LL38 LL37, LL40, LL44
FPA				
FP Mechanics	Improve FPP welding & connectors Increase size for compatibility with flat Win Optimise tile spacing to minimize gaps	Medium Medium Medium	100% 100% 85%	LL24, LL25 Knock-on To address CTAO req.
Window	Iterate to flat window Improve mounting Include optimized coating	Medium Minor Major	100% 80% 85%	LL28, LL29, LL31
Doors	Iterate design such that doors open vertically with a horizontal seam	Medium	90%	LL42
SiPMs	Choose final SiPM technology Develop & test full tiles	Medium Medium	95% 70%	LL02 Knock-on
FP Electronics	Adapt for new SiPM pulse shape Add per-pixel bias control Adapt to revised assembly concept	Major Medium Medium	70% 70% 80%	LL01, LL02. LL06, LL08, LL18, LL34
TM				
TARGET ASICs	Add additional vias to CTC ASIC (keep pin compatible with current design)	Minor	60%	Addressed small performance issue
TM PCAs	Iterate design to accommodate revised SiPMs & FPE	Major	60%	LL02, LL03, LL06, LL07, LL08, LL09, LL10, LL11, LL12, LL13, LL14, LL15, LL16, LL17, LL18
ERA				
Rack	Iterate to use fewer custom parts	Medium	60%	Manufacturability
Backplane	Full design iteration to included XDACQ (and Timing Board) functionality	Major	50%	LL04, LL05, LL48
Slow-Control Assembly	Iterate for compatibility & reliability Final iteration with optimal connectors	Medium Minor	70%	LL46, LL47, LL48, LL44
Timing Board	No changes (or remove – if included in BP)	-	-	-
XDACQ	Remove	-	-	-
Flasher	Iterate to optimize geometry	Medium	40%	LL23
Camera Support Systems				
Chiller Assembly	Iterate chiller (add heating, better stability) Iterate chiller connectors for reliability	Medium Minor	80% 90%	LL36, LL38 Reliability
External Cabling	Change from 12 V to 220 V Change slow control from copper to fibre	Minor Minor	80% 100%	Knock-on Reliability
External Illumination	Design M2 optics & fibre cabling	Medium	45%	LL23
Camera Software	Re-factoring	Major	30%	

7 Technical Design Implementation

This section describes the technical implementation of the SST Camera organised by the PBS. Table 2 indicates the major design features c.f. CHEC-S. The requirements to-which the camera has been designed may be found in [AD3].

Table 2: SST Camera parameters compared to CHEC-S.

Parameter	CHEC-S	SST-Camera
# Pixels	2048	2048
# SiPM Tiles	32	32
Pixels per SiPM Tile	64	64
Active Pixel Size	(3 mm x 3 mm) x 4	6 mm x 6 mm
Tile Size	51.4 mm x 51.4 mm	51.4 mm x 51.4 mm
FoV	8.8°	8.8°
SiPM Technology	S12642-1616PA-50	S14521-1720 (LVR3)
Mass	50 kg	90 kg
Size	500 mm x 500 mm x 500 mm	570 mm x 570 mm x 500 mm
Window Shape	Curved	Flat
Window Material	PMMA	Borofloat / Fused Silica
Window Coating	None	S/N Optimised
Max. Data Rate	1200 Hz	1200 Hz

7.1 Enclosure (ENC)

The ENC is manufactured entirely from machined aluminium pieces with an overall size is 570 mm x 570 mm x 400 mm. This concept is extremely simple to assemble. Mounting eyelets on the top of the Frame provide a lifting point. The ENC includes removeable panels on all sides (apart from the top - to minimise the chance of water ingress), to house power supplies, a heat-exchanger, fans and all connectors. Removable handles can be attached to each panel. To avoid internal condensation and keep the air inside the camera as dry as possible. The breather desiccator prevents moisture from entering the camera when it cools down using desiccant grains, specified for at least 500 heating/cooling cycles before needing replacement. It is difficult to prevent ingress of moisture when assembling/servicing the camera. A one-way purge valve is then used at the end of the assembly or servicing operation, to flush the camera with dry air. The ENC will be finished with a combination of anodising and weather-proof painting. The ENC PBS elements are listed in Table 3. An overview of the Enclosure (ENC) is shown in Figure 11.

Table 3: ENC elements.

PBS Code	PBS Item	Description
SST.4.1.1.1	Frame Assembly	The mechanical frame to which all panels of the ENC are attached. Includes mounting eyelets attached to the top of the frame to lift the camera.
SST.4.1.1.2	Telescope Plate Assembly	The mechanical plate mounted to the rear of the Frame. Forms the mechanical interface to the Telescope Structure and supports the weight of the Camera Unit. The panel faces North with the Telescope is in the Park position at CTA-South.
SST.4.1.1.3	Power Panel Assembly	A panel attached to the Frame containing the power supplies, lightning protection, fuse and all power and data connectors to the camera
SST.4.1.1.4	Heat-Exchanger Panel Assembly	A panel attached to the Frame containing the heat-exchanger, fans and fan-control PCA. Coolant connectors on the outside of the panel form a connection of liquid from the FPA to the chiller return.
SST.4.1.1.5	Fan Panel Assembly	A panel attached to the Frame containing, fans to pull air within the Camera Unit.

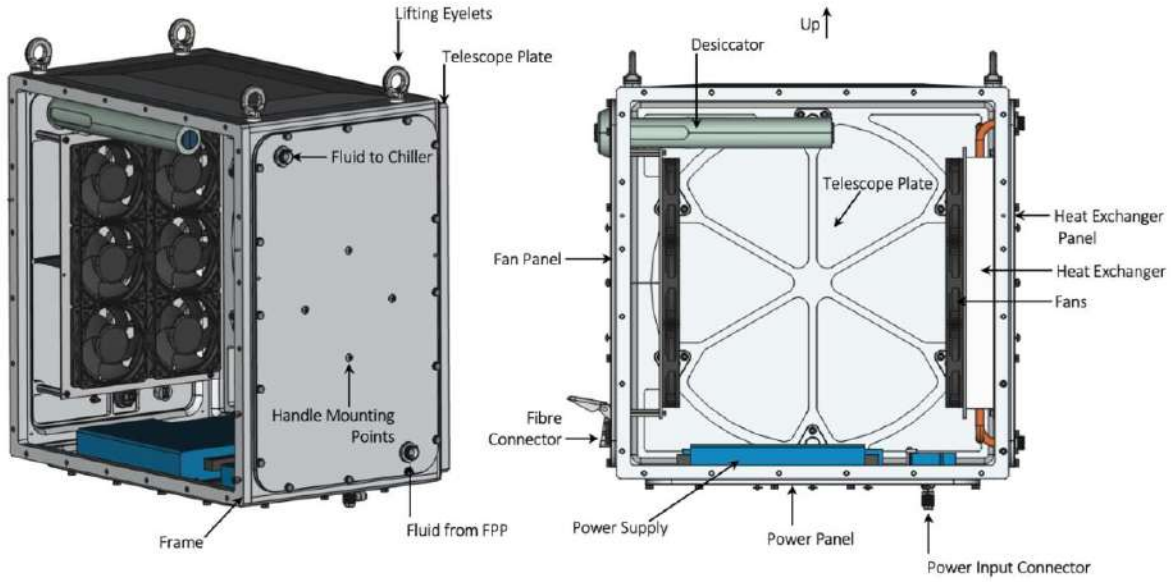


Figure 11: SST Camera Enclosure

7.1.1 Frame Assembly

The Frame is constructed from six machined aluminium pieces welded together (Figure 12). The top side of is closed, and features four mounting eyelets. All other sides are open, and contain blind holes with Helicoil inserts for mounting the ENC panels via M6 screws. Asymmetric dowel pins are provided for alignment and ensure panel orientation. O-rings with vulcanized ends encased in dovetail grooves ensure water-tightness of the seams between Frame and ENC panels. The mounting eyelets are also attached via blind holes with Helicoil inserts to avoid any chance of water ingress. The FPA mounts to the front of the Frame, again via blind holes with Helicoil inserts (an O-ring is present on the FPA side).

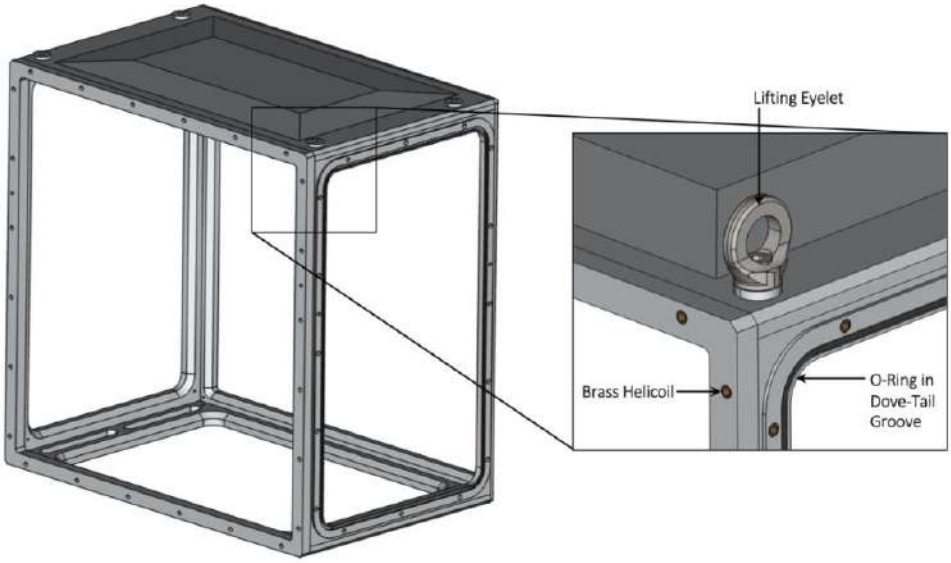


Figure 12: Frame Assembly.

7.1.2 Telescope Plate Assembly

At the rear of the ENC a plate is mounted that forms the interface to the Telescope structure (Figure 13). This plate is a single machined aluminium piece, with six blind holes for attachment to the Telescope. Each hole contains an M12 Helicoil insert. To minimise the thickness of the plate, whilst providing adequate hole depth, some machined "bushes" are used. For a full camera-telescope mechanical interface definition see [AD5].

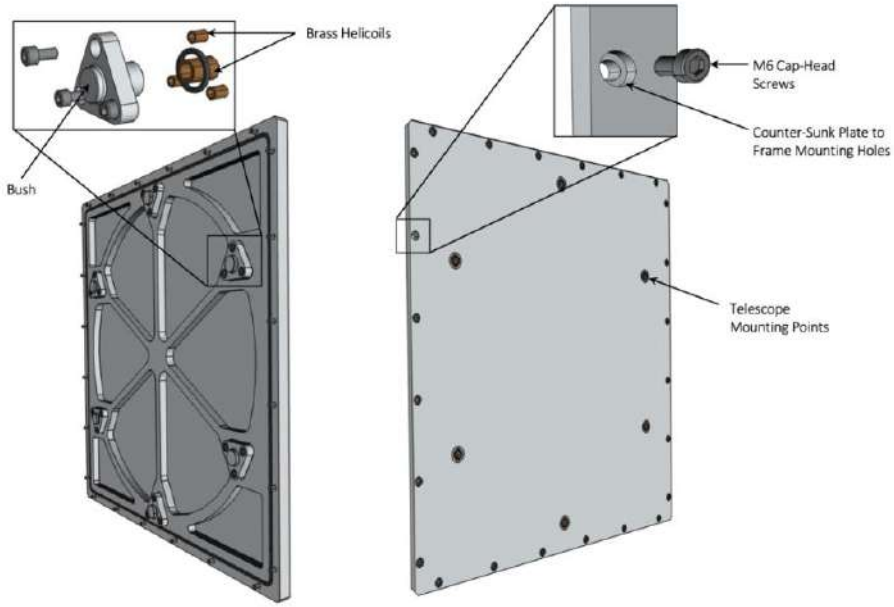


Figure 13: Telescope Plate Assembly.

7.1.3 Power Panel Assembly

The bottom panel of the ENC (Figure 14) will support two conductively-cooled power supply units and electrical protection devices:

- Main PSU: 24V 1500W (MeanWell UHP-1500-24PM), for all the electronics of the camera. This unit has a 95% efficiency, it includes a remote ON/OFF control and PMBus monitoring. It also has a 12V auxiliary power that will keep the Slow-Control Assembly powered, also when the main power is OFF.
- High Voltage PSU: 48V 600W (Meanwell HEP-600-48) for the Photosensor bias voltage. This unit has a 93% efficiency, it includes a remote ON/OFF control and PMBus monitoring. The power provided by this unit exceeds the needs of the SiPM.
- Circuit breakers: (a.k.a. fuses) (Schneider DFCC2V): This is a DIN rail mounted dual fuse holder that can hold standard fuses up to 30A. The fuses can be replaced without removing the holder from the rail. The fuses will prevent damage to the surge arrester in case of very close lightning strike.
- Current surge/spike arrester: (a.k.a. lightning protection) device (DEHN DSH TN 255 FM): This is a 35kA, DIN rail mounted spark-gap-based type 1 and type 2 combined lightning current and surge arrester.

The 220V AC mains power will reach the PSUs from an IP68-rated bulkhead connector (Fischer DEE 104 Z040-8).

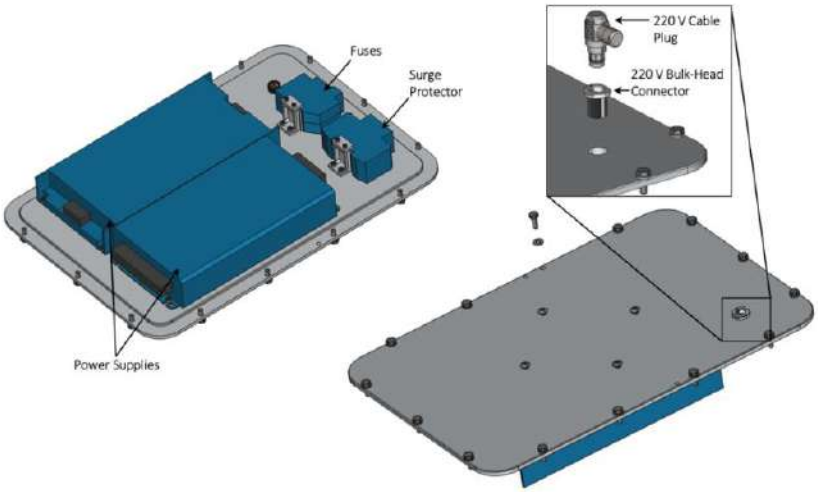


Figure 14: Power Panel Assembly.

7.1.4 Heat-Exchanger Panel Assembly

The Heat-Exchanger Panel Assembly consists of a tray of six 120 mm fans (SanAce 9GA1224P4S0011) coupled to a heat exchanger (Figure 15) mounted to a machined aluminium side panel. The fans will blow air towards the centre of the camera. A small PCB provides PWM control of the fans, and monitors fan RPM and local temperature and humidity. The pipes of the heat-exchanger protrude through the aluminium panel and are terminated on the outside of the camera with quick-release connectors.

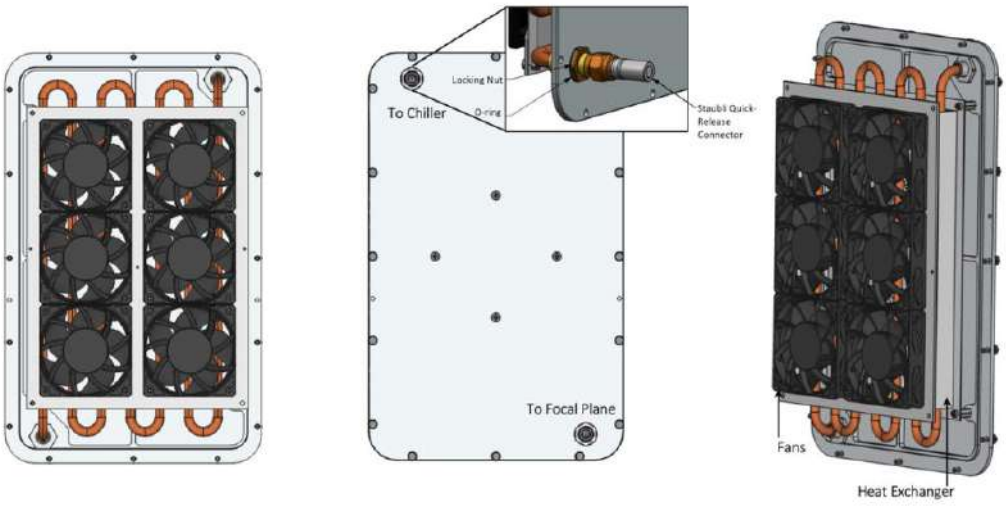


Figure 15: Heat-Exchanger Panel Assembly

7.1.5 Fan Panel Assembly

The Fan Panel Assembly (Figure 16) also contains a tray of six identical fans to the Heat-Exchanger Panel Assembly and PCB for control and monitoring. Fans are oriented to draw air in from the centre of the camera. The machined aluminium side panel sits on the opposite side of the camera to the Heat-Exchanger Panel Assembly. The fan panel also provides a mounting point for:

- Breather - Desiccator (Brownell BLD2233/35)
- Humidity indicator (Brownell BLD10375) (with digital display, active on button touch, to visually check the internal camera humidity without remote connection)
- Fibre optic MTP/MTO connector (Neutrik NO12FDW-A)

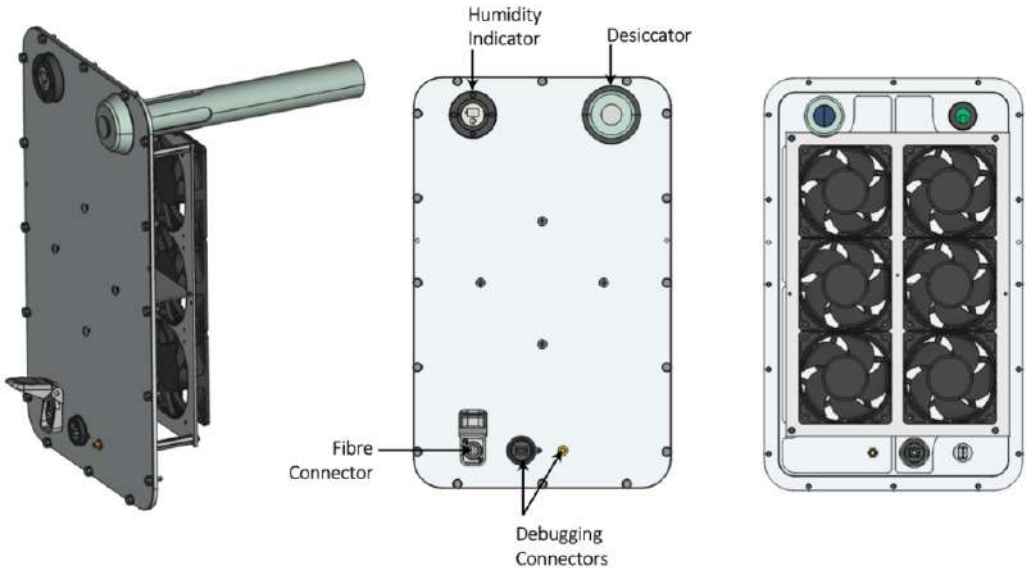


Figure 16: Fan Panel Assembly

7.2 Focal plane Assembly (FPA)

The Focal Plane Assembly (FPA) contains all SiPMs connected to the Focal Plane Electronics Assemblies (FPE) and mounted in the Focal Plane Plate (FPP). The FPP together with a Thermal Break, Transition Plate and smaller mechanical elements form the Focal Plane Mechanical Assembly (FPM). The Window Assembly mounts to the front of the FPP. The FPA includes the doors (and motors). Motor control and position sensor cables enter the camera via grommets on the transition plate. An overview of the FPA is shown in Figure 17, and the ENC PBS elements are listed in Table 4.

Table 4: FPA PBS

PBS Code	PBS Item	Description
SST.4.1.2.1	Focal Plane Mechanical Assembly (FPM)	The mechanical elements of the FPA, consisting of the FPP and all associated elements to support the SiPMs, FPEs, Doors and Window including internal seals, fixtures and fittings and any required for connection to the ERA and ENC.
SST.4.1.2.2	Window Assembly	The coated glass entrance window mounted into a mechanical frame. Attaches to the FPP.
SST.4.1.2.3	Door Assembly	The Camera Unit doors, forming a light-tight seal to the Entrance Window. Mounts to the FPM, and includes two sets of door panels, motor units and proximity sensors. Does not include door control electronics, which are part for the ERA.
SST.4.1.2.4	SiPM Assembly	The SiPM Tile(s) soldered to the SiPM Interface PCA with a heat sink thermally bonded, and a thermal pad added for interfacing to the FPP. 32 per Camera Unit.
SST.4.1.2.5	Focal Plane Electronics Assembly (FPE)	The stack of boards, connectors, heatsinks and cables providing 64 pixels of adjustable bias voltage and preamplification. Sits between the SiPMs and the TMs and terminates with a spring-loaded board to allow TMs to be connected blindly. 32 per Camera Unit.

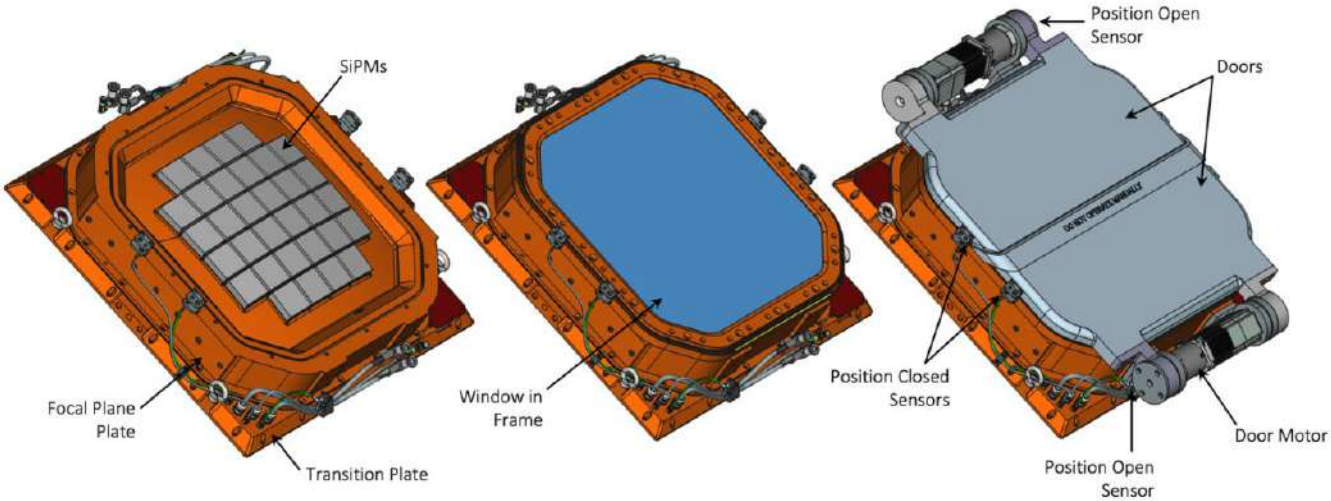
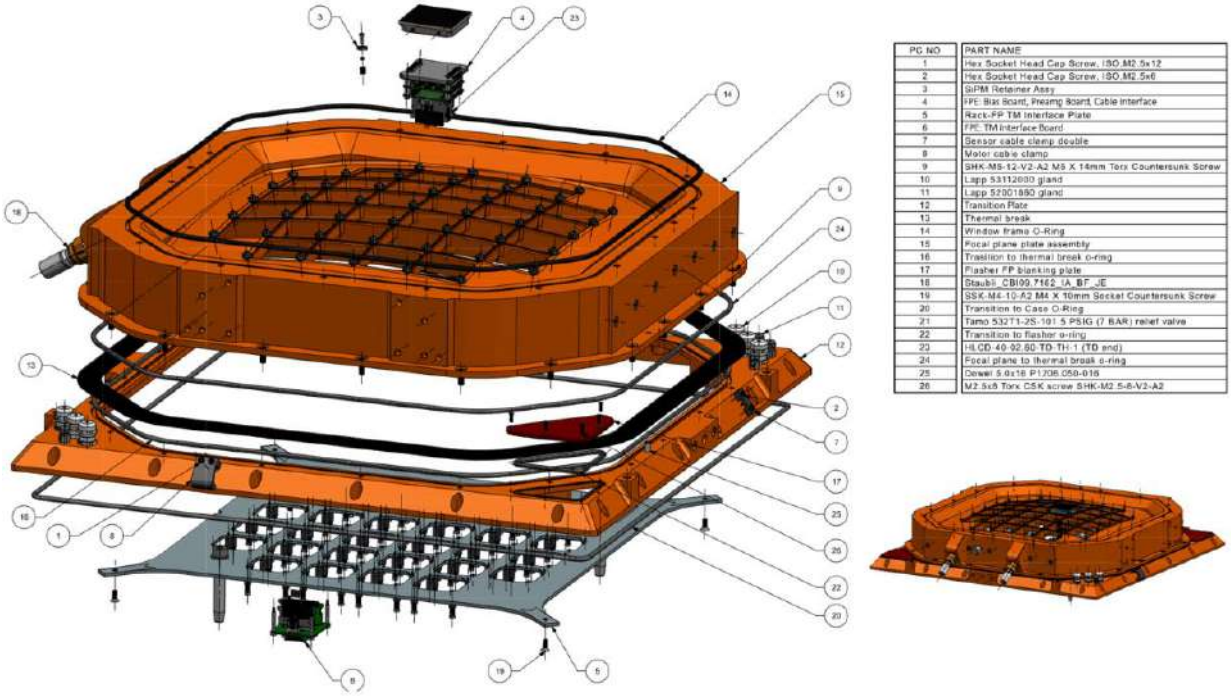


Figure 17: The FPA at various stages of integration.

7.2.1 Focal Plane Mechanical Assembly (FPM)

This FPM is shown in Figure 18, together with a single SiPM & FPE. The FPM consists of the Focal Plane Plate (FPP) measuring 510 mm x 510 mm, a Thermal Break, Transition Plate, Rack Interface Plate and fittings / seals. The FPP is a convex grid of square holes supporting the FPE and SiPM assemblies. The FPP domed shape allows the flat surfaces of the SiPM sensors to be tiled along the curvature of the focal plane defined by the telescope Schwarzschild-Couder optics.



PG NO	PART NAME
1	Hex Socket Head Cap Screw, ISO,M2.5x12
2	Hex Socket Head Cap Screw, ISO,M2.5x6
3	SiPM Retainer Assy
4	FPE: Bias Board, Preamp Board, Cable Interface
5	Rack-PP TM Interface Plate
6	FPE TM Interface Board
7	Sensor cable clamp double
8	Motor cable clamp
9	SHK-M5-12-V2-A2 M5 X 14mm Torx Countersunk Screw
10	Lapp 53112080 gland
11	Lapp 52001880 gland
12	Transition Plate
13	Thermal break
14	Window frame O-Ring
15	Focal plane plate assembly
16	Transition to thermal break o-ring
17	Flasher FP blanking plate
18	Staubli_CBI00.7162.1A..BF..JE
19	SSK-M4-10-A2 M4 X 10mm Socket Countersunk Screw
20	Transition to Case O-Ring
21	Tamo 5327T1-2S-101.5 PSIG (7 BAR) relief valve
22	Transition to flasher o-ring
23	HLCD-40-02.80-TD-TH-1 (TD end)
24	Focal plane to thermal break o-ring
25	Dewar 5.0x18 P1706.050-016
26	M2.5x8 Torx CSK screw SHK-M2.5-8-V2-A2

Figure 18: FPM Assembly breakdown.

The FPP structure is hollow. Liquid circulates as shown in Figure 19 to cool the SiPMs and FPE. The FPP is sealed on the rear side by electron-beam welding a plate into the machined cavity. Thermal contact between the cold FPP ribs (4.5 mm drill holes along the 510 mm long, 7 mm wide ribs) and the FPE is enhanced using pre-cut thermally conductive silicone pads. Both inlet and outlet coolant pipes and fittings are placed on one side of the plate with ruggedized straight quick-release connectors. A pressure relief valve is fitted to the FPP to prevent pressure build up following disconnect from the flexible cooling hoses with chilled liquid inside the FPP.

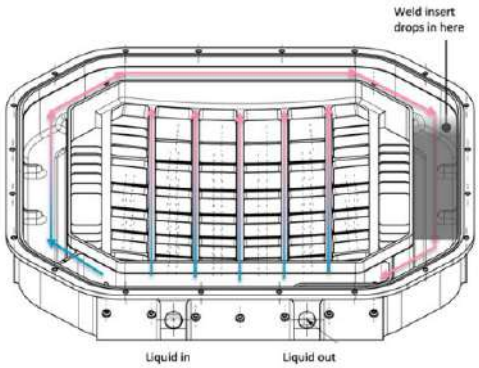
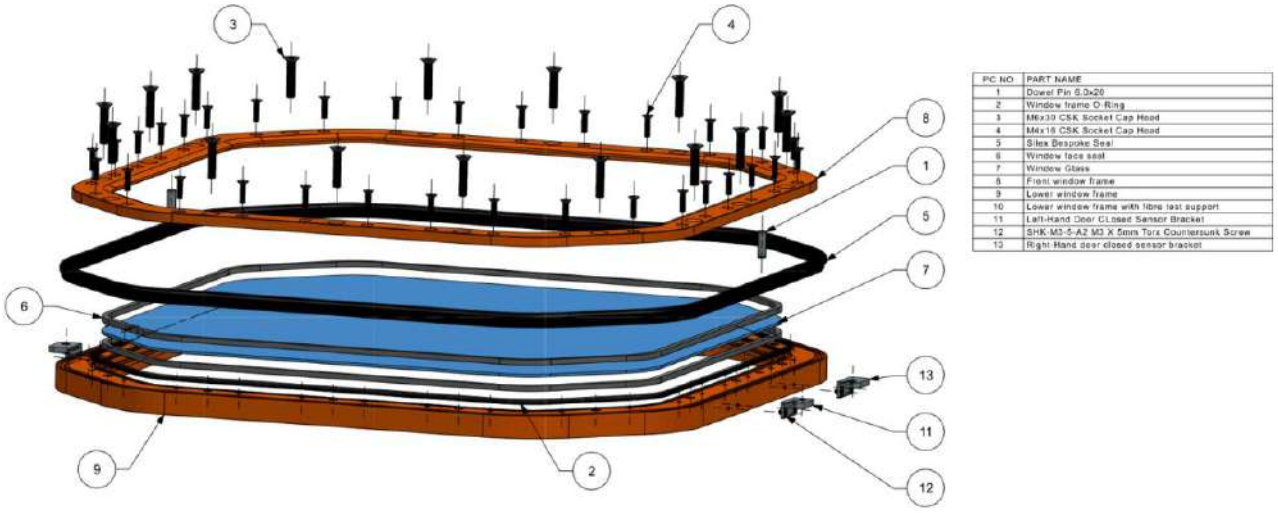


Figure 19: Liquid flow though the FPP.

The FPP is attached to the Enclosure by the Transition Plate via a thin Thermal Break plate, made from composite material with low thermal conductivity. This plate prevents heat exchange between the FPP and the Enclosure. The Rack Interface Plate is a simple flat plate with a grid of square holes, designed to support the TARGET Module Interface Assemblies. The system features spring-loaded screws to allow the FPA to be fully integrated, for the TARGET Modules to be attached from the rear, and then the Backplane to be added as a final step (see Section 10).

7.2.2 Window Assembly

The Window Assembly seals the camera and protects the SiPMs and electronics during observations and blocks the majority of the NSB photons whilst providing good transmission of Cherenkov light to all pixels with little or no-vignetting. The Window Assembly is shown in Figure 20 and consists of a two-piece window frame, and the window itself.



PC NO	PART NAME
1	Dowel Pin 6.0x20
2	Window frame O-Ring
3	M6x30 CSK Socket Cap Head
4	M6x18 CSK Socket Cap Head
5	Silex Bespoke Seal
6	Window face seal
7	Window Glass
8	Front window frame
9	Lower window frame
10	Lower window frame with fibre test support
11	Left-Hand Door CLosed Sensor Bracket
12	SHK-M3-5-A2 M3 X 5mm Torx Countersunk Screw
13	Right-Hand door closed sensor bracket

Figure 20: The Window Assembly.

The entrance window of CHEC-S was curved (made from PMMA and uncoated). A curved window can sit at a uniform distance from the SiPMs, and must only extend across the active pixel area. However, a curved window is difficult to manufacture and coat. A flat window can instead be used, but must extend past the active SiPM area to not shadow the outer SiPM pixels from light arriving at large angles. Figure 21 shows the distribution of angles onto the window from the M2 mirror (left), and the corresponding acceptance cone required at the window to prevent shadowing of the outer pixels. The increase in window size, and corresponding support mechanics size, comes at the cost of increasing the shadowing caused by the camera from light leaving M1 and arriving at M2, as well as an increase in overall camera mass due to the increased dimensions, but is within acceptable limits. The flat window size is then a trade-off between minimising the shadowing of outer SiPM pixels whilst not creating too much of a detrimental effect on the effective area of the telescope.

Figure 21 (left) shows the SST effective area as function of field angle for window apertures of 360 mm to 450 mm. The black and red lines correspond to directions across the camera towards the corner and edge respectively. The extent of the SiPMs (i.e., the active camera area), is marked by the vertical dashed lines. A window size of 430 mm (indicated by the thick curves) results in no shadowing of the outer SiPM pixels. There is therefore no need to make the window aperture any larger than this. Whilst the CTA effective area requirement (5 m^2) is met down to significantly smaller window sizes, the

effective area quickly becomes none-uniform across the camera due to the aforementioned shadowing of the outer pixels. Therefore 430 mm is taken as the baseline choice for a window aperture size.

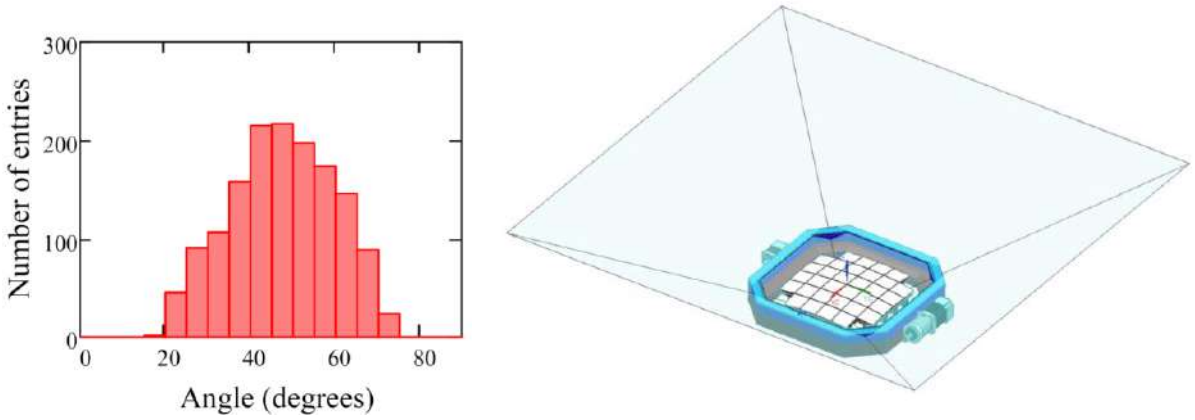


Figure 21: Left: Incidence angles onto the window from the SST optics. Right: Window Frame Acceptance Cone.

The window will be produced from either Borofloat33 or quartz / fused silica (depending on cost and availability). The mechanical window frame is designed to accommodate glass thickness in the range 1.75 mm to 2.00 mm (but may be adapted to any thickness > 1.00 mm). The outer 4 mm of the glass will be trapped between environmental seals, and so does not require coating. The seals will be made of neoprene and bonded to both window and frame. A thickness of 2 mm has initially been chosen to provide a good balance between mechanical robustness and transmission. The window is flat and square in shape with the corners cut-off; it is 442 mm from long side to long side (see Figure 22 (right)). See Section 10.1.2 for a brief description of the process used to mount the window glass in the frame.

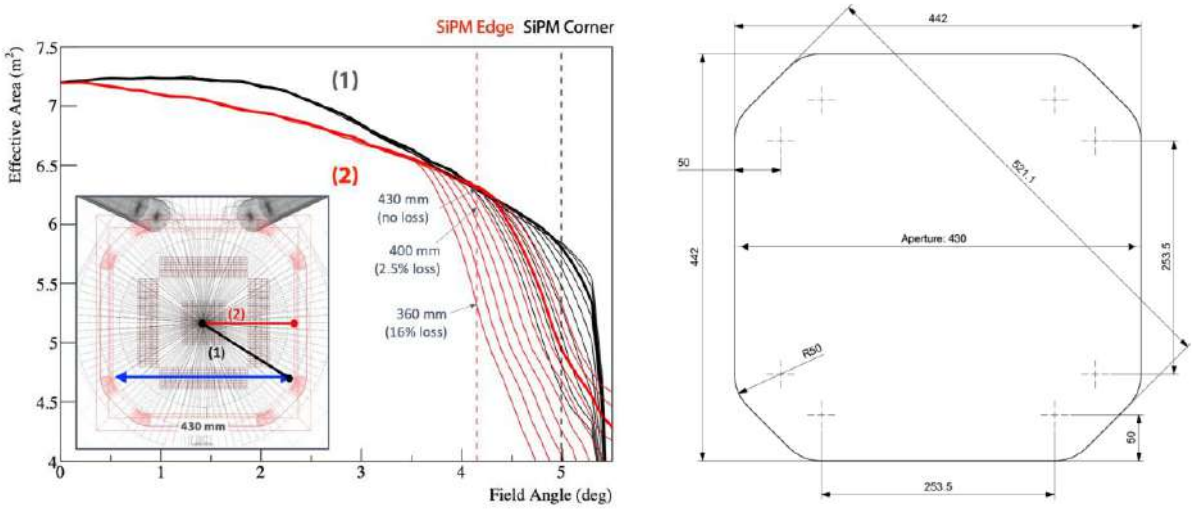


Figure 22: Left: Effective area vs. field angle for window apertures from 360 mm to 450 mm. Right: Window glass dimensions.

The window feature a 79-layer SiO_2/HfO_2 coating applied to the outside (front), to maximise Cherenkov light transmission and minimise the influence of NSB. The window transmission is shown in Figure 23 for a selection of incidence angles. The transmittance is in good agreement with the simulations, in general exceeding expectations. The transmittance at 300 nm is 73% at 20° angle of incidence, rising to 80% at 45° before falling to 75% and 72.5% at 50° and 60° respectively. At 350 nm, the transmittance is over 85% at all but a 60° angle of incidence, where it is 80%. At a 20° angle of incidence, the

transmittance at 557 nm (where there is a strong oxygen emission line in the NSB) is 90%. This falls rapidly to 45% at 45°, 34% at 50° and 22% at 60°.

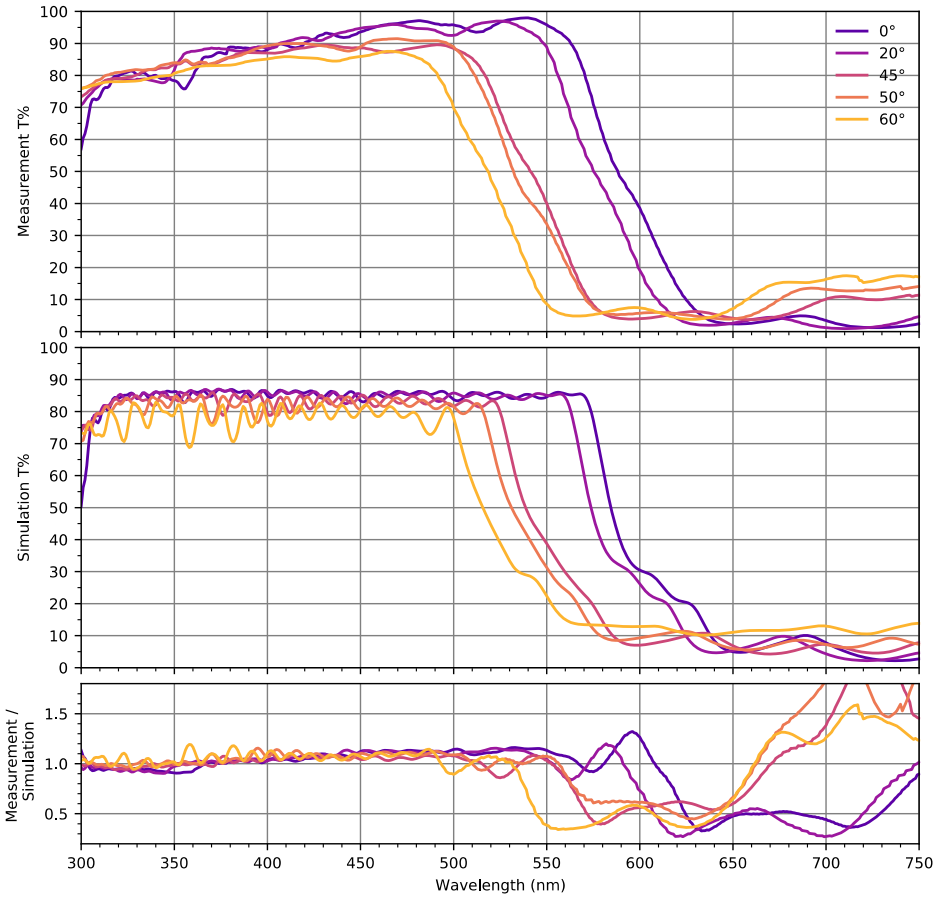


Figure 23: Window transmission measurements (top) and simulations (middle). Note: measurements are made on quartz.

7.2.3 Door Assembly

The Door Assembly consists of the doors themselves (a.k.a. lids) and the motors, gearboxes, hinges, seals, proximity sensors and encoders allowing the doors to be opened and closed and their position to be known at all times[1]. The Door Assembly design is illustrated in Figure 24.

The seam between the two doors runs horizontally, and the doors move towards the top and the bottom enclosure panel when opening. The panels are made of aluminium, with isogrid ribs to increase rigidity. Their open edge is slanted to avoid seal rubbing. The top panel edge has a stepped seam cover with a D-shaped seal running below it, secured to the panel by screws at its two ends. This will prevent rainwater ingress on the window, and protects the seal from light exposure. The doors seal against the Window Assembly via a seal mounted on the outer edge of the upper window frame.

The motors are high-torque (1.87 Nm) Nanotec AS5918L4204-EB+GP56-T2 stepper motors. They are coupled to Nanotec GP56-T2-20-HR planetary gearboxes providing a gain ratio reduction of 20:1. The motors have sufficient torque to allow the lid to be closed in the presence of winds of up to 40 km/h as per CTA requirement and to sufficiently compress the custom D-seal, ensuring a good seal.

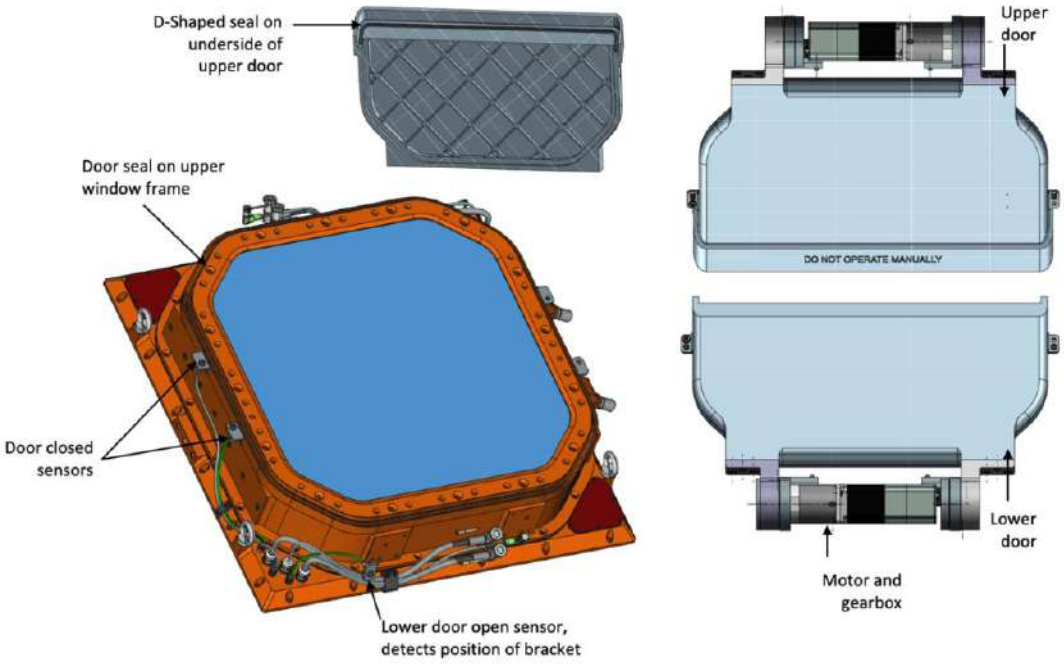


Figure 24: Door Assembly overview.

The motors each include a brake and a position encoder. The brake ensures that the doors stay in position without the need for power to the motors. Four Pepperl and Fuchs proximity sensors (NBB1-4GM22-E0) are placed to determine the fully open and closed positions and triggered by set screws. The open position sensors are located near the middle of the camera, whereas the closed position sensors are mounted to detect set screws in the rotating door brackets.

[1] Note, the motor controllers & FW are part of the SCA (see Section 7.4.3).

7.2.4 Silicon Photomultiplier (SiPM) Assembly

SiPMs have been chosen as a photon sensor for the SST Camera because of their compact nature, low cost per channel, high photon detection efficiency and robustness against a high photon-rate environment. They nevertheless come with challenges including: optical cross-talk, gain dependence on temperature and NSB illumination level, and sensitivity to higher wavelengths than PMTs. The use of the latest SiPM technology, liquid-cooled focal plane, Cherenkov-optimised window coating, and built-in illumination flashers, are used to mitigate these issues for the SST Camera.

The SiPM Assembly is shown in Figure 25 and consists of the SiPM tile and heatsink ([RD5]). The tile is provided by Hamamatsu (HPK), whilst the heatsink is machined in-house from aluminium and thermally bonded to the SiPM tile upon delivery. The heatsink is clamped to the FPP as part of the FPA AIT procedure (see Section 10.1.2). In this way the interface board connectors do not need to provide any significant retention force. Sil pads on the heatsink provide good thermal contact to the FPP.

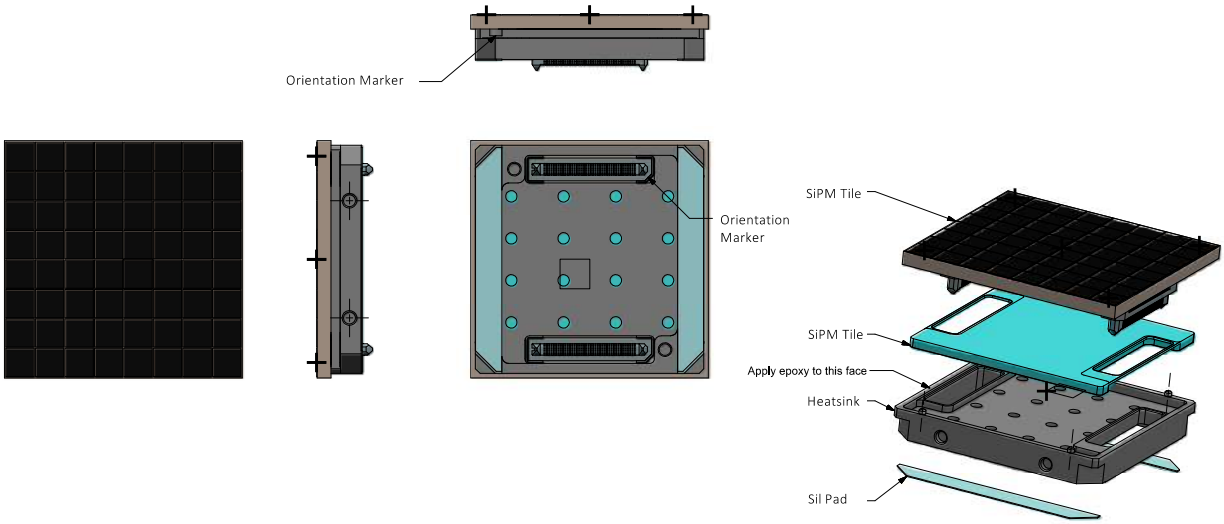


Figure 25: SiPM Assembly.

Figure 26 shows the interface PCB, which provides:

- 64 (i.e., per pixel) bias resistors (1 kOhm, 1% tolerance, rated to 150 V) and filtering capacitors (100 nF, rated to 250 V), routed individually to multi-pin connectors.
- Four PT1000, 1-wire, temperature sensors, with an accuracy of up to +_0.1° C. Each PT1000 is individually to the TARGET Module.
- A 1-wire serial ID chip, also routed to the TARGET Module.

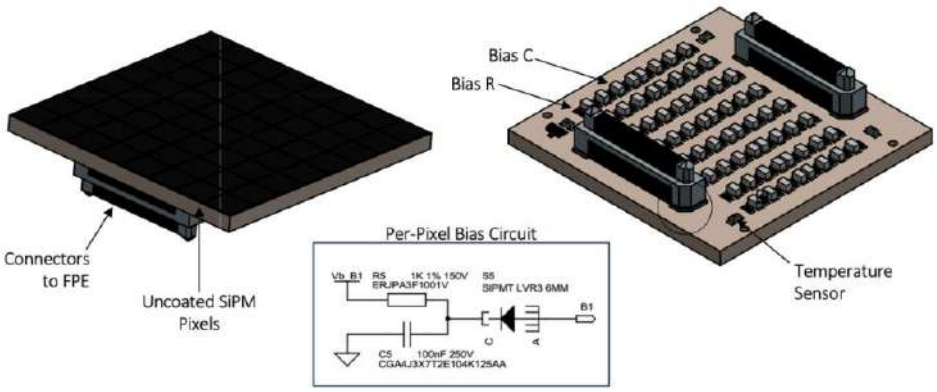


Figure 26: SiPM tile, including interface PCB with per-pixel bias circuit.

7.2.4.1 Pixel, Tile & Focal Plane Geometry

The SiPM pixel and tile geometry are shown in Figure 27. Each tile consists of 64, uniformly spaced, pixels. The focal plane geometry including gaps between active area of pixels on adjacent tiles is shown in Figure 28. Table 5 summarises the pixel, tile and focal plane geometric properties.

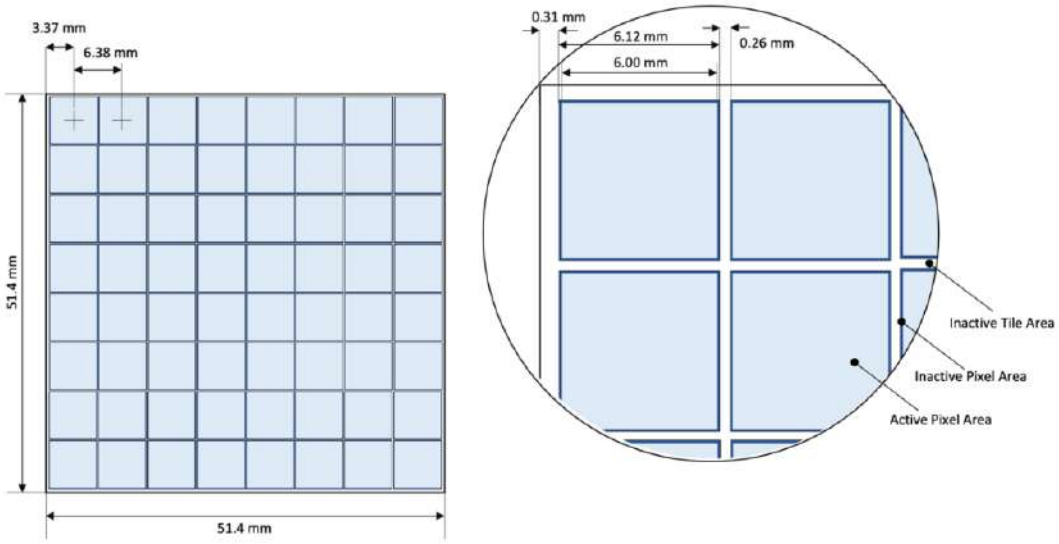


Figure 27: SiPM pixel and tile geometry.

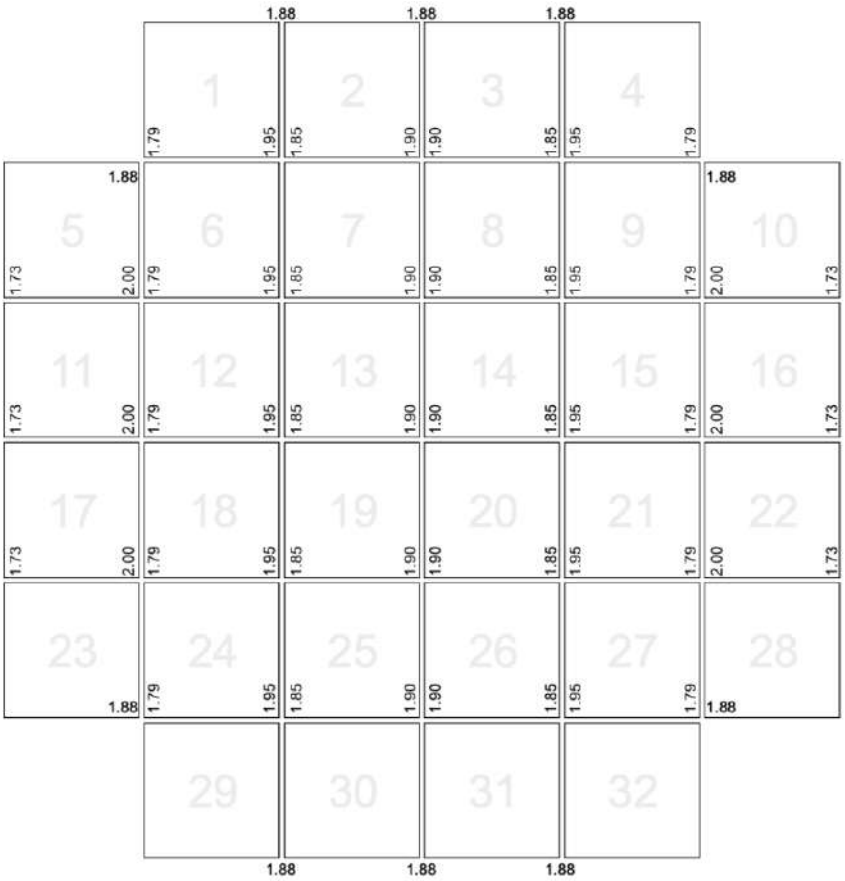


*Figure 28: Focal plane layout showing 32 SiPM tiles. Numbers show the gaps between the adjacent **active** pixel areas on tile edges and are rotated to indicate the direction of the gap.*

Table 5: SiPM pixel, tile and focal plane geometric properties.

Parameter	Value	CTA Requirement
Pixel		
Active pixel size	6 mm x 6 mm (0.16°)	<0.23°
Physical pixel size	6 .12 mm x 6.12 mm	
Tile		
Tile Size	51.4 mm x 51.4 mm	
Gap between pixels within tile	0.26 mm	
Gap between pixels and tile edge	0.31 mm	
Pixel pitch	6.38 mm	
Tile fill factor	87.2%	
Focal Plane		
No. tiles per camera	32	
Minimum gap between active area of pixels on adjacent tiles	1.63 mm	
Maximum gap between active area of pixels on adjacent tiles	2.00 mm	<2.16 mm
Implied FoV	8.8°	>8.0°
Implied fully instrumented FoV	7.8°	>6.8°
Camera fill factor	84.6%	

7.2.4.2 SiPM Technology

Several SiPM candidates and pixel sizes were considered, tested, and discussed in detail prior to deciding on the choice of SiPM technology for the SST Camera (see [RD6] for details). The chosen SiPM technology "LVR3" from HPK, with 50 µm microcells and no protective coating (single pixel: S14520-2246, tile part number: S14521-1720). LVR3 offers higher PDE and lower optical cross talk than the nearest competitor, LCT5 (see Figure 29). Uncoated is preferred due to the lower optical cross talk, but presents challenges in handling. As a fallback option, coated SiPMs could be adopted post-ECAM without changes to the rest of the camera. A cell size of 70 µm would offer a higher PDE than 50 µm (corresponding to the difference in geometric fill factor of 82% vs 74%), but the coated 70 µm option has worryingly high optical cross-talk (ruling out the fallback option just mentioned). LVR3 also has the downside of a pulse that is difficult to shape whilst retaining a useable signal-to-noise ratio. Whilst this is manageable for 50 µm cells, and is successfully addressed with the preamp (see Section 7.2.5) and TARGET Module shaping circuit designs (see Section 7.3.1), it is an even greater challenge for 70 µm cells. The SiPMs will nominally be operated at an overvoltage (V_{ov}) of 5.9 V.

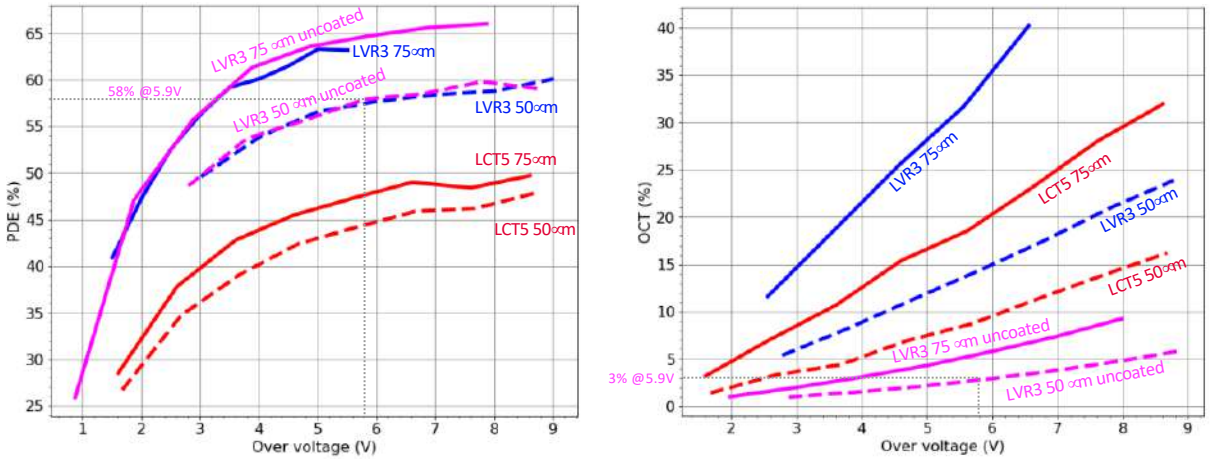


Figure 29: Candidate SiPM PDE and OCT measurement (U. Nagoya). SiPMs feature a 300 µm coating unless otherwise stated.

Table 6 shows the primary characteristics of the chosen SiPMs with comparison to CHEC-S, some of which discussed below.

Table 6: SiPM properties.

Parameter	CHEC-S	SST Camera	Unit
Part	S12642-1616PA-50	S14521-1720	
Pixel area	3.0 x 3.0 x 4	6.0 x 6.0	mm^2
Microcell size	50	50	µm
Coating thickness	300	0 (no coating)	µm
Spectral response range	220 to 900	220 to 900	nm
Peak PDE	40	55	%
Breakdown voltage (V_{br})	68 +/- 5	38 +/- 3	V
Prompt OCT probability	~ 35	~ 3	%
Pixel Fill factor	74	74	%
V_{br} Temperature Dependence	60	34	mV/°C

Dark Counts: In silicon, there is a finite probability for carriers to be generated by thermal agitation leading to a single p.e. event rate, known as the Dark Count Rate that forms a source of noise for the SiPM. The expected NSB level in nominal operating conditions for the SST is expected to be ~40 MHz p.e. per pixel. The Dark Count Rate for the 6 mm LVR3 SiPM is 3 - 6 MHz per pixel, and is therefore a negligible additional source of noise.

Optica Cross talk: OCT occurs when a secondary (IR) photon is created in the avalanche of an incoming progenitor photon. The OCT rate is expected to be proportional to the number of electron-holes pairs produced in an avalanche (i.e., the avalanche gain), which is proportional to the product of cell capacitance and over voltage. The OCT rate tends to increase with higher photon detection efficiency (PDE). Furthermore, the device geometry and the coating thickness are important in determining the propagation properties of crosstalk photons, and therefore the likelihood of OCT. We can consider the possible OCT mechanisms as shown in Figure 30.

- **Path A:** Photons propagate through the silicon substrate, reflect off the backside and hit a neighbouring cell. OCT occurring with a time delay of less than ~8 ns as contributing to the "prompt" OCT and the later faction as "delayed" OCT.
- **Path B:** Photons propagating directly to neighbouring cells, effectively instantly, and contributing to the "prompt" OCT. This component has largely been eliminated by the inclusion of trenches.
- **Path C:** Photons can reflect off the SiPM coating and fire a neighbouring cell, contributing to the "prompt" OCT.
- **Path D:** Photons can also bounce back from a coating and hit the same cell again, which does not contribute to the OCT as the cell is in recovery.
- **Path E:** Photons can also bounce off the SiPM coating into a neighbouring pixel. This can also occur via the camera entrance window. We call this "reflected" OCT, and is considered separately to "prompt" and "delayed" OCT.

As shown in Table 6 the total level of "prompt" OCT is significantly reduced compared to CHEC-S, to a level where it is no longer a concern. This is due, in part, to the use of uncoated SiPMs, removing path C. The "delayed" OCT level is independent of the SiPM coating, and thought to be entirely due to path A. For 50 µm cells a level of ≈ 12% is expected. Whilst it could be suppressed by implanting a barrier between the avalanche region and the bulk this will likely not happen for CTA. However, delayed OCT has been explored in simulations and does not show any detrimental effects on basic trigger or intensity resolution performance beyond that expected by increasing the NSB level. As noted, path E is still

possible via reflection from the camera entrance window and characterisation of this “reflected” OCT is underway.

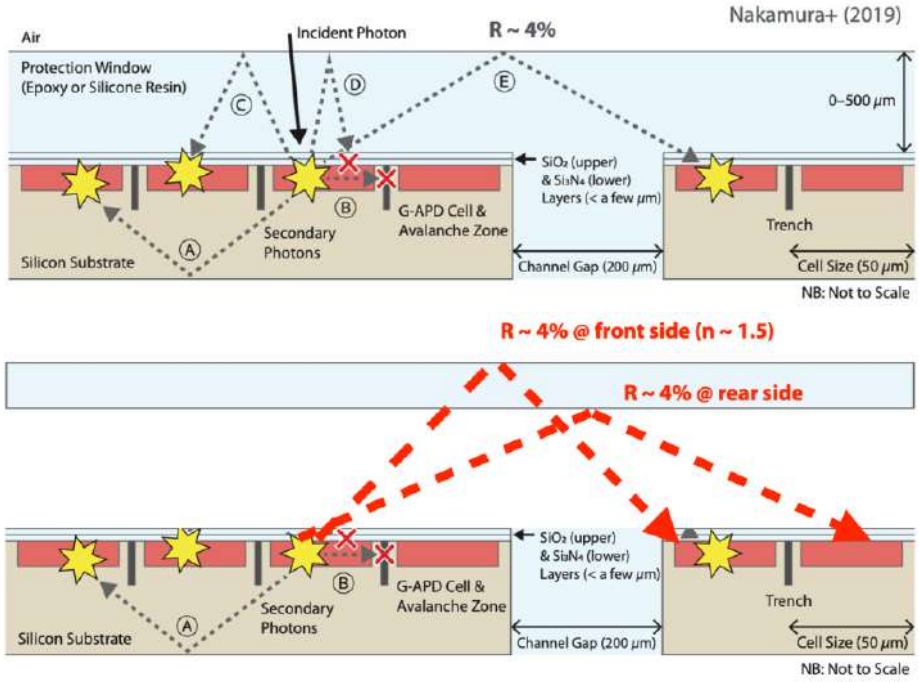


Figure 30: Schematic view of possible propagation paths of infrared photons causing optical cross-talk (top) and together with the camera window (bottom).

7.2.4.3 SiPM Power Dissipation

The SiPM gain depends on temperature. To operate at a stable gain, the SiPMs are, therefore, thermally coupled to the liquid-cooled Focal Plane Plate. SiPM heating increases with the average (DC) illumination level, and therefore power consumption, which is self-limiting due to the passive safety feature provided by a current-limiting resistor in the bias circuit (see Figure 31, top). Each SiPM tile could dissipate a maximum of 11.5 W under the most extreme illumination (>10 GHz NSB p.e. per pixel levels, c.f. the nominal 40 MHz in dark skies). Under the same conditions the 64 preamplifier channels per SiPM tile will dissipate ~5 W, making the Focal Plane Plate cooling requirement ~530 W under extreme conditions. However, this level of power dissipation in the focal plane is never planned to occur across large fractions of the focal plane for more than a fraction of a second, due to active SiPM bias voltage control on the FPGAs of the Target Modules. A more reasonable maximum for operation may be taken as: 80% of pixels at 1 GHz (corresponding to the maximum illumination level required for operation of the SST by CTAO) and 20% at complete saturation (due to very bright stars), which leads to ~200 W at the focal plane. Under normal conditions (under 100 MHz NSB per pixel), each SiPM tile is expected to draw ~0.3 W and each set of 64 preamplifier channels ~3.5 W, implying a cooling capacity of ~120 W at the focal plane is required. The Focal Plane Plate thermal control system has been specified such that only a small increase in SiPM temperature occurs with a total continuous load exceeding that expected under normal conditions to ensure that no recalibration is needed to take into account variations in SiPM parameters (such as gain and PDE) that can occur with temperature (see the next sub-section for details).

7.2.4.4 *The Influence of NSB*

The use of a current-limiting resistor prevents the SiPMs from being damaged under extreme illumination conditions. However, such a resistor placed in series with every SiPM pixel, creates an unwanted effect. As the NSB increases, the current flowing through the SiPM + R_{bias} circuit increases. Since the bias voltage supply to the circuit is constant, this increase changes the voltage drop across the SiPM (i.e., V_{ov} drops). As Gain, PDE and OCT all depend on V_{ov}, these also all drop. A change in overvoltage of ~500 mV over 1 GHz increase in NSB is expected.

The SiPMs will be operated at a nominal V_{ov} = 5.9V, on a PDE "plateau" (see Figure 29), such that no significant changes occur with the overvoltage drop associated with NSB increases (55% PDE decreases to ~54% PDE with a 500 mV drop). The OCT change relative to the pulse amplitude is also insignificant (i.e., 3% OCT decreases to 2.5% OCT with a 500 mV drop). The Gain change dominates, dropping by ~20% over a 1 GHz NSB change, as shown in Figure 31. In normal, and even reasonably bright, conditions no additional calibration is needed (i.e., a drop in pulse height of ~5% from dark to 200 MHz NSB is acceptable). However, to ensure the best possible knowledge of the gain at all times, and to correct for drops up to the maximum required observing conditions, regular flashes of a constant and stable medium brightness will be interleaved with normal data taking at a rate of 10 Hz from the Flasher Assembly (see Section 7.5). In addition, an absolute measure of the NSB will be provided for every pixel in parallel to normal data taking via the "slow" acquisition chain (see Section 7.3.4).

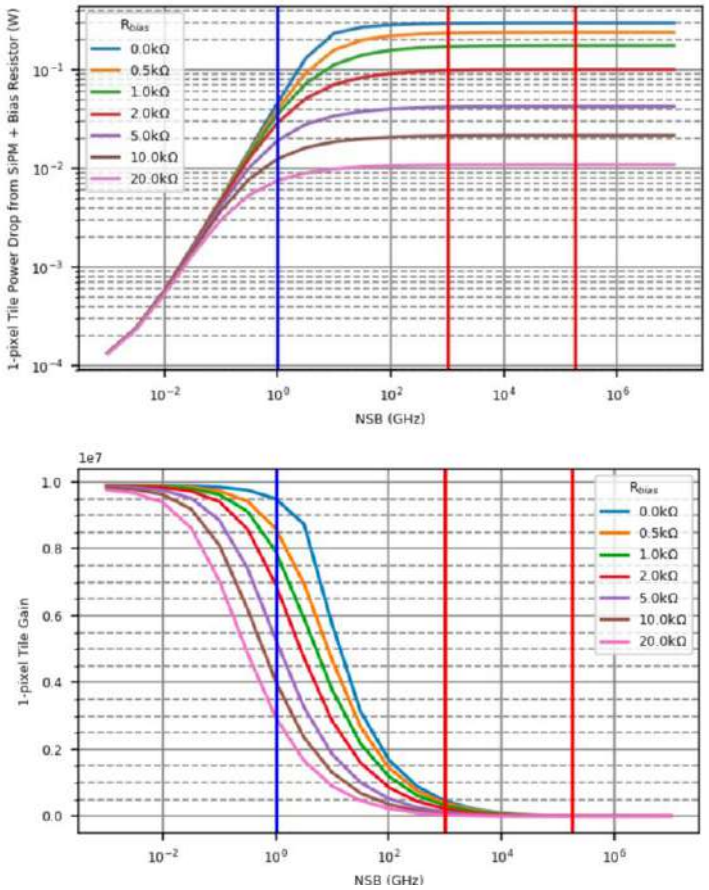


Figure 31: Top: Expected power dissipation from a single 6 mm x 6 mm SiPM pixel as a function of NSB level. Bottom: Expected gain drop as a function of NSB level. A bias resistor (R_{bias}) of 1 kOhm has been chosen. The vertical blue line indicates the maximum expected operating conditions for the SST.

7.2.4.5 SiPM Handling

The use of uncoated SiPMs introduces a risk of damage during handling. This is mitigated with: dedicated tools, assembly areas and procedures at several stages of camera integration. At all points of handling, ESD precautions will be followed and gloves will be worn.

- SiPM tile transport. SiPM tiles will be shipped from HPK and packed appropriately. Upon arrival, they be handled only as is essential and will be stored in a humidity-controlled environment.
- Heatsink attachment. The SiPM tiles arrive with Kapton tape on the active surface. This will remain in place until FPA integration, and provides crucial protection for heatsink attachment.
    - The Fisnar adhesive robot (also use to mount the window in the frame and the preamplifer heatsinks) will be used to apply thermally conductive epoxy adhesive Multlcomp MC002964 to the border face of the heatsink.
    - The tile is placed by hand onto the heatsink, following markers to ensure orientation.
    - Very light pressure is applied to the front surface of the tile using a custom soft-faced compression tool.
    - The epoxy is cured following the appropriate temperature profile.
    - Avoiding pressure on the silicon, the assembly is placed face-down into a potting jig.
    - The heatsink cavity is filled by injecting thermally conductive filler Bergquist TGF3500LVO trough all holes, using the Fisnar glue robot for accuracy and repeatability. Any excess filler is removed from the rear of the heatsink.
    - The thermal pads are applied to each heatsink foot.
    - The SiPM tile is placed in a dedicated storage and transport case, with humidity control.
- Integration into the FPA. Enclosing the SiPMs in done prior to full camera assembly at an institute with the required facilities. A clean room is not required, but a controlled environment free from obvious dust with dedicated assembly jigs are needed. A tool has been developed and will be used to avoid touching the SiPM tiles by hand. Once secured in the focal plane, the SiPMs are protected by the entrance window and FPP. After this point, it is not envisaged that the FPA will be opened until maintenance is required. The FPA will be stored and transported to the camera integration site in a dedicated case with humidity control.
- Camera AIT. Camera integration will take place in a room with temperature and humidity control that is regularly cleaned. The SiPMs will not be handled directly.
- Maintenance. No on-site replacement of SiPMs is envisaged. The FPA is treated as a low-level line-replaceable unit, and shipped off-site to be diagnosed and SiPM tiles replaced if necessary. Full spare FPAs will be provided to CTAO for use in corrective maintenance.

The option of using coated SiPMs also remains open, pending evaluation of the handling requirements of uncoated tiles and the evaluation of the trade-off between ruggedness and performance.

7.2.5 Focal Plane Electronics (FPE) Assembly

The Focal Plane Electronics (FPE) Assembly provides the mechanical, electrical, and thermal interfaces for the SiPM Assembly and serves to mechanically position and support the photosensors accurately in the camera focal plane. There are 32 FPE Assemblies in the camera, one for each SiPM tile, mounted on the Focal Plane Plate. Each FPE Assembly consists of:

- **Preamp Assembly:** Connects directly to the SiPM Assembly to shape and buffer SiPM signals.
- **Bias Assembly:** Generates controllable bias voltages for each pixel of the SiPM tile.
- **Cable Interface Assembly:** A passive interface board.
- **Cables:** Used to go from the curved focal-plane surface to the planar TARGET Module rack.
- **TARGET Module Interface Assembly:** A second passive interface board mounted on springs to the Rack Interface Plate (see Focal Plane Mechanics) that connects on one side to Cables, and on the other side the TARGET Modules.

An overview of the FPE, showing the Preamp Assembly, Bias Assembly, Cable Interface Assembly with SiPM Assembly attached is shown in Figure 32.

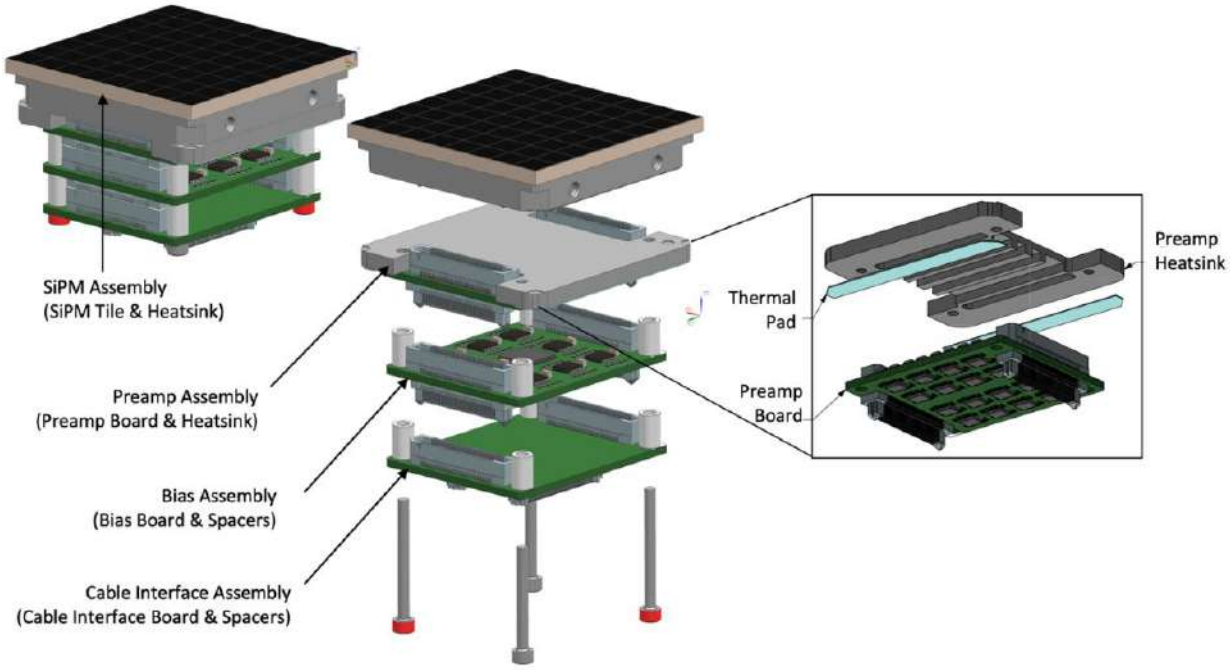


Figure 32: FPE, showing the Preamp Assembly, Bias Assembly, Cable Interface Assembly with SiPM Assembly attached.

The **Preamplifier Board** comprises an array of operational amplifiers configured as transimpedance amplifiers which convert the SiPM current pulse to an amplified, DC-coupled voltage signal. The preamplifiers are situated as close as possible to the SiPM tile to minimize the effect of parasitic inductance which would be detrimental to the downstream signal shaping electronics. The limited space available on the preamplifier PCB necessitates a quad package op-amp which also limits the choice of available devices. The primary requirements for the op-amp are a sufficiently high bandwidth ~400 MHz for the 10 ns wide pulses required by the trigger channel coupled with suitably low noise for single p.e. resolution. The device chosen is the Ti LMH6722 which satisfies the requirements for low power dissipation in combination with a suitably economical cost for the 2048 channels per camera.

The Preamplifier Board uses the same quad op amp as CHEC-S in a transimpedance configuration to convert the SiPM current pulse to a voltage pulse. The SiPM performance since the CHEC-S devices has improved dramatically with higher PDE, lower crosstalk, and lower dark count rate being achieved with the selected LVR3-5060VN devices. However, the SiPM signal fall time is longer by a factor x2.5 meaning that for the same gain, the pulse amplitude is reduced by the same factor, placing more emphasis on the signal-to-noise ratio which influences the charge resolution accuracy. A pole-zero cancellation circuit has implemented as part of the transimpedance feedback network on the Preamplifier Board (see Figure 33) to allow an extra shaping stage to be implemented in the analogue shaper on board the TARGET Module to help offset this issue. The SiPM pulse shape arrives at the Preamplifier Board with a width of ~120 ns, and leaves with a width of ~6 ns. After further shaping and integration on the TARGET Modules, the pulse has a width of ~10 ns and an improved signal-to-noise ratio. For further details of the pulse shaping, and expected performance, see [RD7].

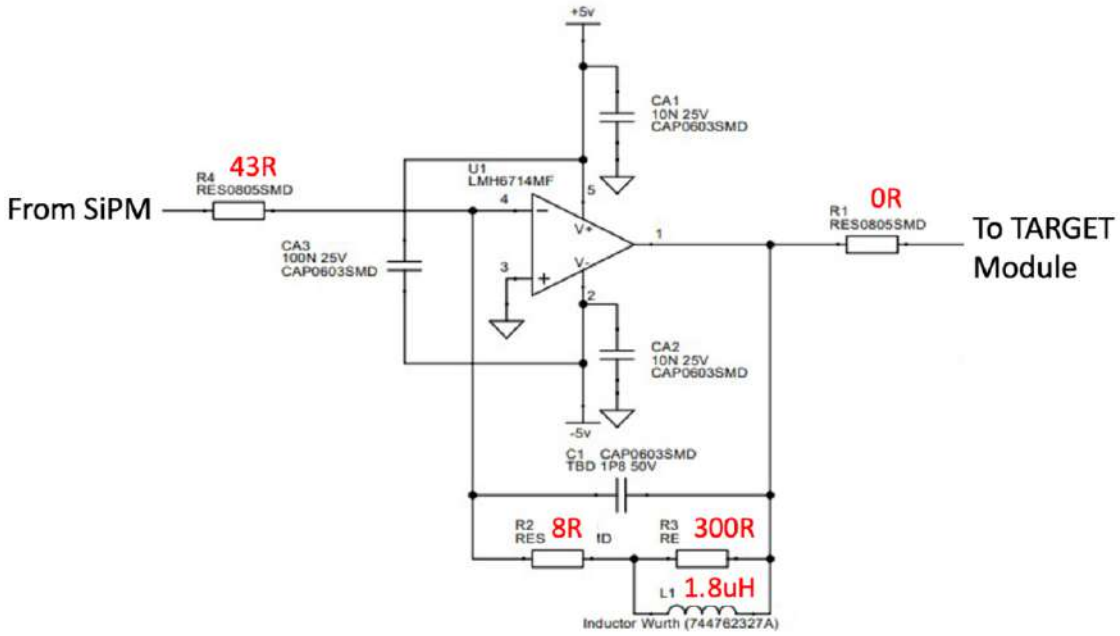


Figure 33: A single channel of the Preamplifier Board op-amp & zero-pole circuit.

The **Bias Board** generates 64 independently controlled bias voltages, one for each pixel. This is an improvement over the CHEC-S scheme which used 16 voltage regulators located on the TARGET power board to generate independently controllable bias voltages for each super-pixel of 2 x 2 pixels, limiting the ability to fully gain match the CHEC-S SiPM responses. The SST Camera design still uses the original 16 bias supplies from the TARGET Modules as inputs, allowing these to be independently trimmed for optimisation of the power dissipation, but uses a high-voltage op amp per pixel to reduce this to the desired SiPM pixel bias. Two 32-channel DACs provide the precision voltage used by the op amp to generate the per-pixel bias voltage. The bias voltage for each pixel can be set with 16-bit (0.8 mV) resolution between 0 and 48 V, and the typical break-down voltage of a pixel is ~38 V.

The **Cable Interface Assembly**, **Cables** and **TARGET Module Interface Assembly** provides the power and signal interfaces between the SiPM, FPE and the TARGET Module (see Figure 34). Cables are used accommodate the variable distance and tilt between the curved focal plane and the planar rack housing the TARGET module. The TARGET Module Interface Assembly utilises a sprung architecture which allows the TARGET Modules to be inserted from the back of the camera and mated with FPE power and signal connectors after the latter are installed. This ensures proper connection without too much stress on the connectors.

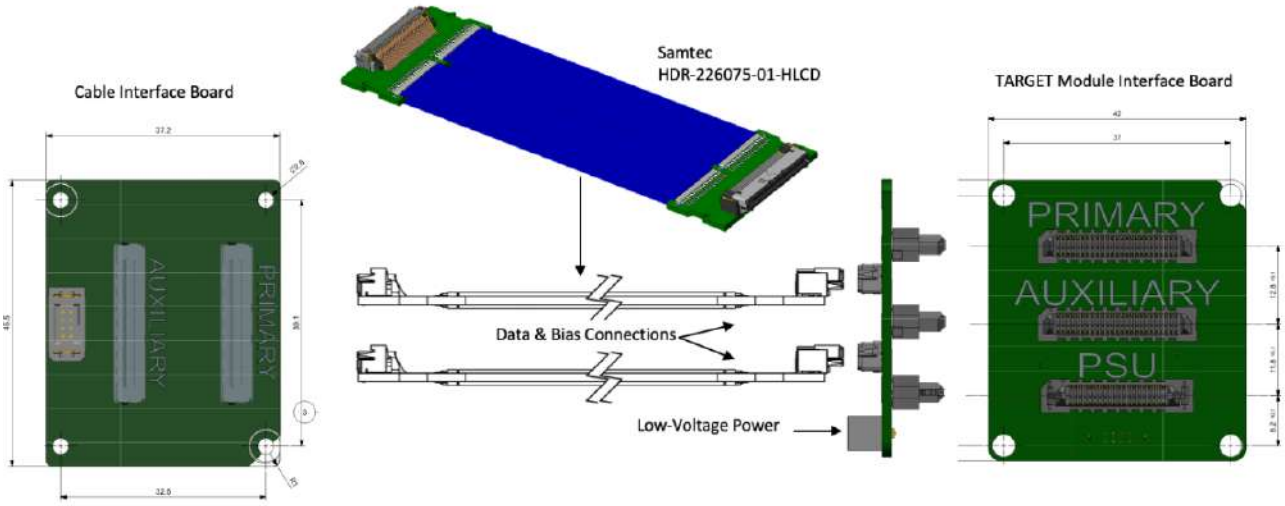


Figure 34: FPE Cable Interface Board, Cables and TARGET Module Interface Board.

The Preamplifier and Bias Boards will be made of a heat-conductive PCB material (ceramic-filled laminate. The interface boards be connected with Samtec 0.50 mm Razor Beam high-speed hermaphroditic connectors and coax cable assemblies, ensuring very good connector retention. The rear of the preamp heatsink features thermal pads, that improve the thermal contact when mounted to the FPP. The heatsink itself is bonded to the preamp board using thermally conductive epoxy adhesive (Mulllcomp MC002964) via a Fisnar glue dispensing robot to achieve repeatable results and fast manufacture. The heat dissipation of the FPE design is much improved with respect to CHEC-S (see simulation results in [RD8] and Figure 35). This ensures stable and reliable operation, better gain performance, better calibration and longer lifetime. It also improves the EM shielding, leading to less electronic noise and better overall camera performance.

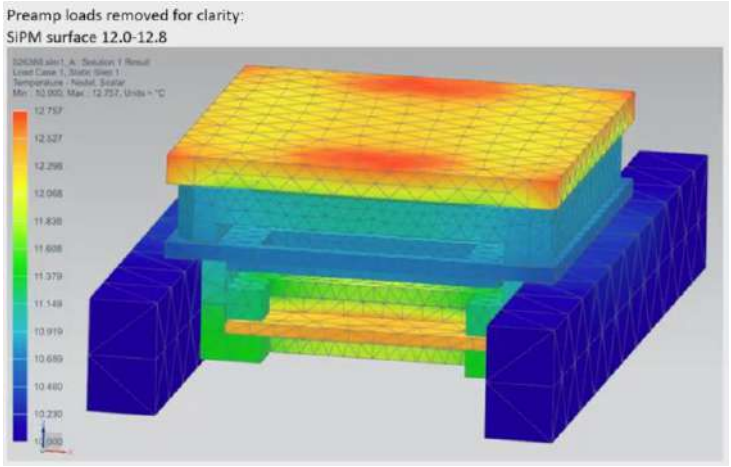


Figure 35: FEM simulation of an SiPM tile and part of the FPE Assembly connected to the Focal Plane Plate, showing temperature gradients. The colour scale goes from 10 to 12.7 °C. The coldest parts are the FPP ridges.

7.3 TARGET Modules

The TARGET (TeV Array Readout Electronics with GSa/s sampling and Event Trigger) Modules consist of three interconnected PCAs (Primary, Power and Aux Board) onto which the TARGET ASICs are placed. The TARGET Module PBS breakdown is shown in Table 7, and CAD model in Figure 36.

Signals enter the Primary (Prim.) and Aux. boards from the FPE, mapped via one Samtec cable (carrying 32 sets of pixel signals) each. The Prim. and Aux. boards then contain an analogue shaping stage for each pixel, before routing the signal to two paths. A DC-coupled slow path with ADC, is used to monitor the brightness of stars and the NSB level in the camera. A fast path is AC-coupled to TARGET sampling (CTC) and TARGET trigger (CT5TEA) ASICs located on each board. Each ASIC accepts 16 channels of input and so four are required on each TARGET Module (two per Prim. and Aux. Board) to accommodate the 64-pixel SiPM tile. Digital data output from the slow-signal ADCs and all four ASICs are routed to a Xilinx Series 7 Artix FPGA housed on the Prim. Board. The FPGA provides control and monitoring of all elements of the TARGET Module and provides the control, monitoring and raw-data link to the Backplane via an Aurora link. Trigger ASICs output 1st-level camera trigger signals directly to the Backplane (16 per TARGET Module, 512 per camera). The Power Board provides power conditioning, internal voltage generation and sequencing, using 24 V and 48 V (for SiPM bias voltage) input via the Backplane from the camera power supplies. A single connector at the rear of the TARGET Module on the Prim. Board forms all connections to the Backplane.

Table 7: TARGET Module PBS

PBS Code	PBS Item	Description
SST.4.1.3.1	TARGET ASICs	The TARGET sampling and trigger ASICs, 4 each per TM, 128 per camera.
SST.4.1.3.2	TM Primary PCA	The primary TM board, to be populated with two CTC and two T5TEA ASICs. Contains control FPGA. Connects to the TM-Interface-Assembly and BP.
SST.4.1.3.3	TM Auxiliary PCA	The auxiliary TM board, to be populated with two CTC and two T5TEA ASICs. Mounts to the TM Primary PCA. Connects to the TM-Interface-Assembly.
SST.4.1.3.4	TM Power PCA	The TM board containing all power generation and monitoring components for the other TM PCAs. Mounts to the TM Auxiliary PCA and accepts 24 V and 48 V (SIPM power) input from the BP via the TM Primary PCA along with control signals.
SST.4.1.3.5	TM Fixtures and Fittings	The fixtures and fittings used to assemble the three TM PCAs into a module.
SST.4.1.3.6	TM Firmware	The Firmware to the TMs, running on the FPGA of the TM Primary PCA.

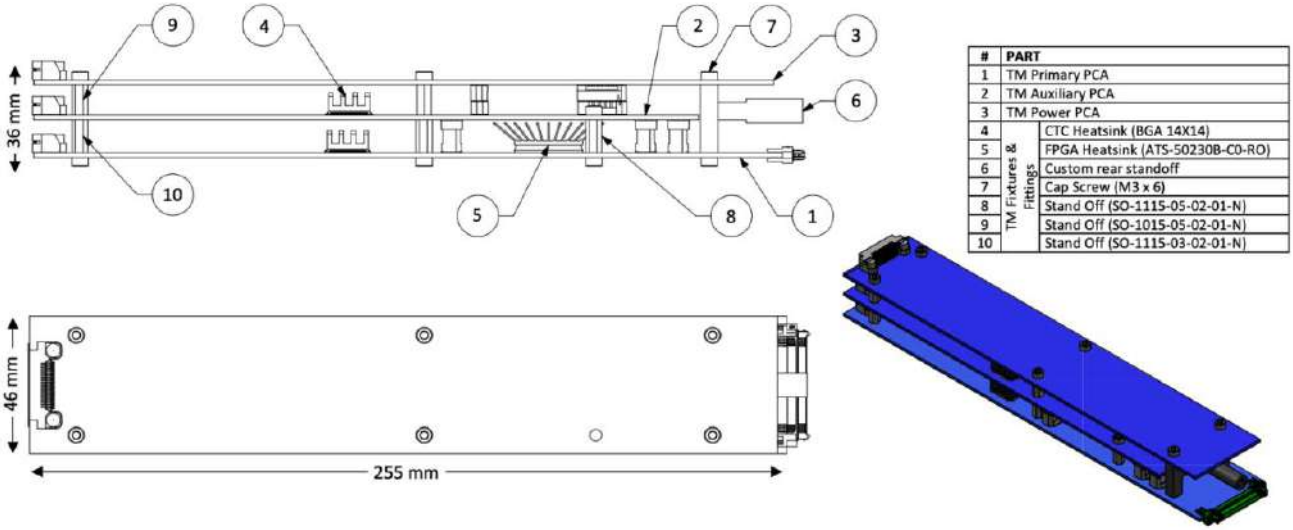


Figure 36: TARGET Module CAD overview (note: dimensions are approximate only).

7.3.1 TARGET Module Analogue Shaping

Each channel includes a shaper circuit as shown in Figure 37, reconfigured from the design used for CHEC-S, using the same op amps and a similar number of components to maintain the footprint size. The Preamplifier Board feeds the negative-going amplified and shortened SiPM to the pulse shaper circuit located on the TARGET Module via 50 Ohm coaxial Samtec ribbon cables. The input to the first op-amp stage terminates the cable with a 50 Ohm load. The signal is inverted and amplified in the first stage op-amp and fed to the slow and fast signal chains. The slow chain comprises a 1 ms integrator and additional summing resistor fed from a 2V5 reference voltage and op-amp buffer stage on the power board. The summing resistor is required to offset the slow output voltage which otherwise has a -300 mV offset (outside the slow ADC range - a known problem with CHEC-S). The fast signal chain initially utilized a second order Sallen-Key filter to implement a 2-stage integrator to improved signal to noise. This circuit has been simulated in LTSpice and produced the necessary pulse shape and width. The output of the second stage is coupled into the 50 Ohm PCB traces to the ASICs, with the 50 Ohm termination at the ASIC providing x2 attenuation, thus limiting the maximum shaper voltage to slightly less than the ASIC saturation level. When coupled with the preamplifier and SiPMs operated at nominal overvoltage (5.9 V), a pulse of FWHM ~10 ns and amplitude of 3.2 mV/pe is obtained at the ASIC inputs.

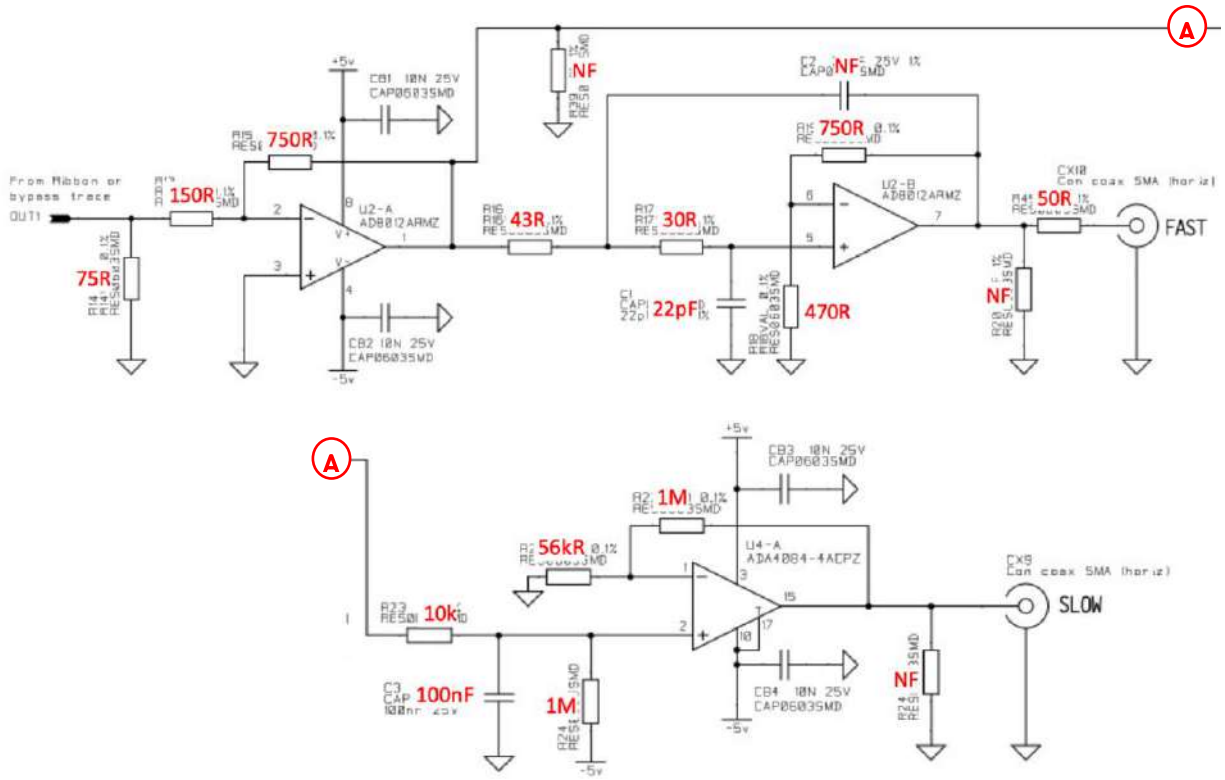


Figure 37. Shaper circuit diagram.

7.3.2 TARGET Module Sampling & Digitisation

The TARGET-CTC ASICs, are responsible for sampling and digitisation of the waveforms. Figure 38 demonstrates the digitisation process for a single ASIC. A 64-capacitor cell array samples the readout from the fast signal line in a "ping pong" fashion (one 32 set is sampling while the other is writing) at a rate of 1 GSa/s. The charge is then transferred to a 16384-capactitor array (of which 4096 are used in the SST Camera) for the intermediate storage and buffering of the samples. Following and instruction to readout, digitization is performed by Wilkinson ADCs over a range of ~0-2 V, with 12-bit resolution, at a configurable lookback time in the storage array. The number of samples digitised is settable in blocks of 32, and for the SST Camera is typically set to 128 (corresponding to 128 ns of readout). This waveform generation is illustrated in Figure 39.

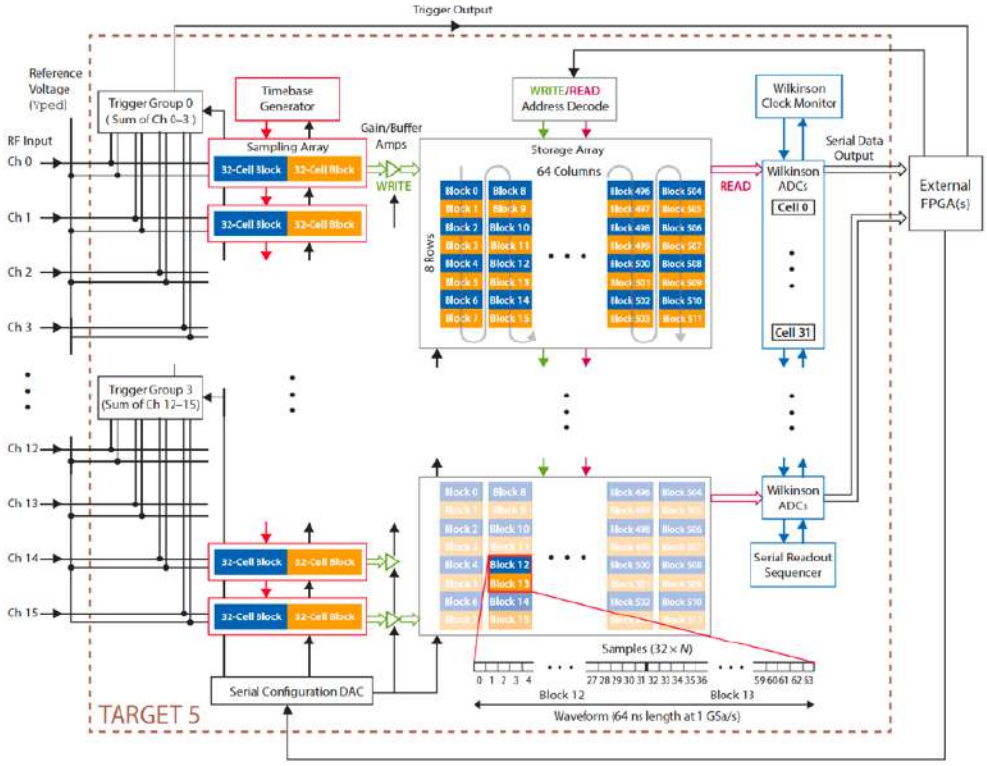


*Figure 38: Functional block diagram of the TARGET-5 ASIC [RD9]**Error! Reference source not found.**, also applicable to the TARGET-CTC ASIC.*

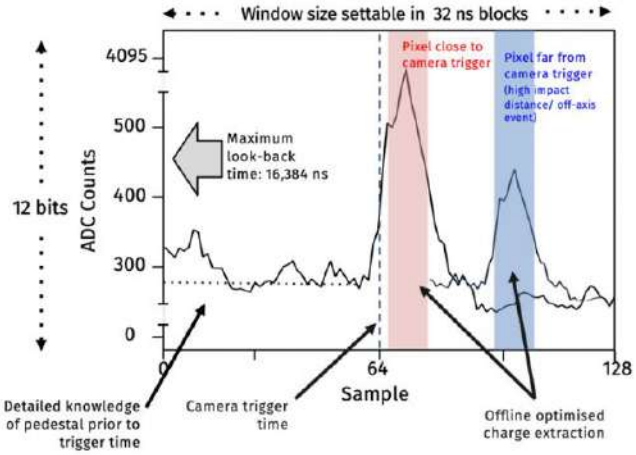


Figure 39: Overview of the waveforms obtained from a single camera pixel

7.3.3 TARGET Module Trigger & Readout

The TARGET-CT5TEA ASICs produce the first level threshold when the analogue sum of the fast signal line from a group of 4 pixels (forming a "superpixel") exceeds the configurable threshold, as demonstrated in Figure 40. Each LVDS (Low-Voltage Differential Signal) trigger line is sent to the Backplane for camera-level trigger determination. Following a camera-level trigger, a signal is sent to the TARGET Module FPGAs and the TARGET-CTC ASICs are instructed to readout. Digitisation occurs as described above, and the resulting event data (i.e., 64 waveforms per TARGET Module), and unique identifier, are serialized by the FPGA and output to the Backplane via Aurora connection (which is also used for all monitoring and control of the TARGET Modules).

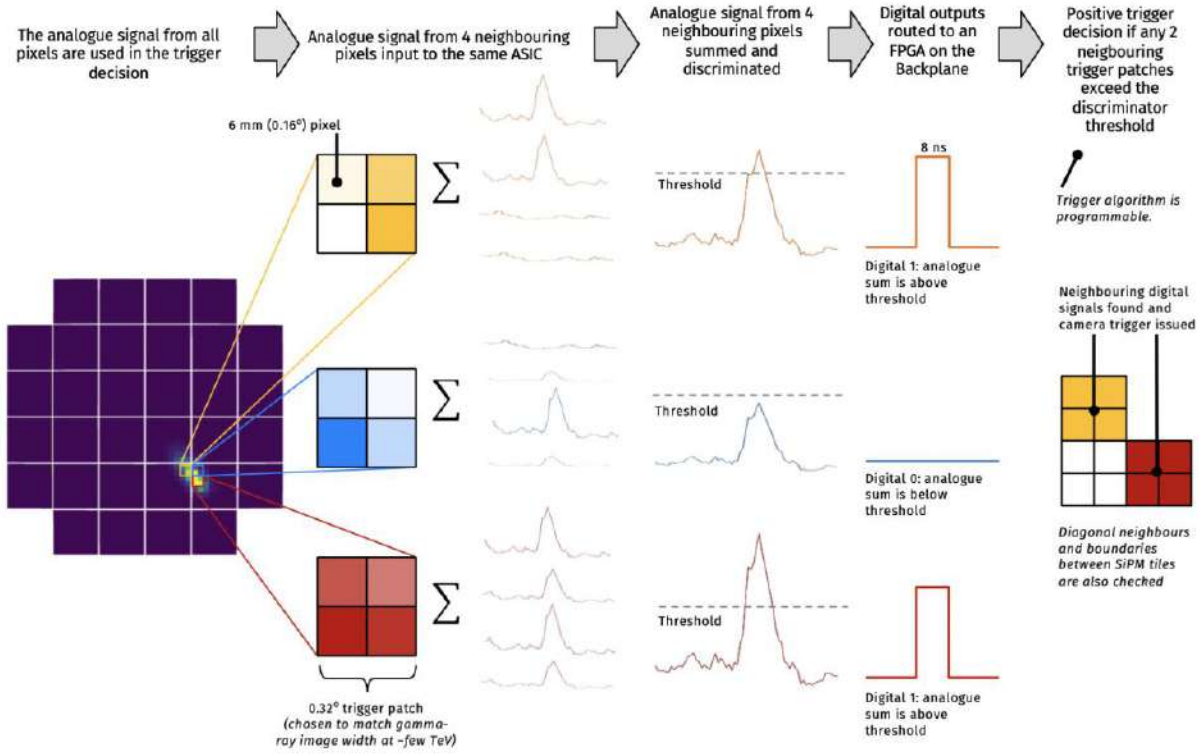


Figure 40: Overview of the camera trigger scheme.

7.3.4 TARGET Module Slow Signal Acquisition

The slow signal chain provides integration and digitisation of all channels continuously (i.e., independently of the trigger scheme) on timescales useful for determining the camera NSB level and star positions (i.e., for astrometry). Frames (i.e., all pixels) are output from the FPGA at 10 Hz, each frame has an integration time / exposure of 1 ms. The chain is configured to allow determination of the NSB level from ~1 MHz p.e. rate per pixel (below the dark count rate of the SiPMs) up to several GHz (by which point the SiPM response saturates due to the voltage drop across the bias resistor). A typical SST NSB field in dark skies corresponds to ~40 MHz p.e. rate per pixel. These rates correspond to a range of approximately Mag 7 down to Mag 3 stars. At Mag 7, approximately 10 – 30 stars per FoV are expected (sufficient for astrometric calculations).

7.4 Electronics Rack Assembly (ERA)

The Electronics Rack Assembly consists of Backplane, Timing Board and Slow Control Subassembly, mounted on a Mechanical Rack with Cabling between components and to the ENC (see Table 8 and Figure 41).

Table 8: ERA PBS

PBS Code	PBS Item	Description
SST.4.1.4.1	Mechanical Rack Assembly	The mechanical rack that houses 32 TMs, the Backplane, Timing Board and Slow-Control Assembly. Including all cable attachment points and standoffs, screws and washers for PCB attachment.
SST.4.1.4.2	Backplane PCA	The Backplane PCA and associated firmware. Attaches to the rear of the mechanical rack. Accepts power from the SCA, and has fibre optical connection to the ENC.
SST.4.1.4.3	Slow-Control Assembly	The Slow Control Assembly (SCA) is responsible for power distribution and control to the Camera Unit components and environmental monitoring (temperature and humidity).
SST.4.1.4.4	ERA Cabling and Connectors	All cables and connectors routed between components on the ERA and forming interfaces to/from the ERA, attached to the Rack.
SST.4.1.4.5	Timing Board	The Timing Board PCA and associated firmware. Attaches to the mechanical rack.

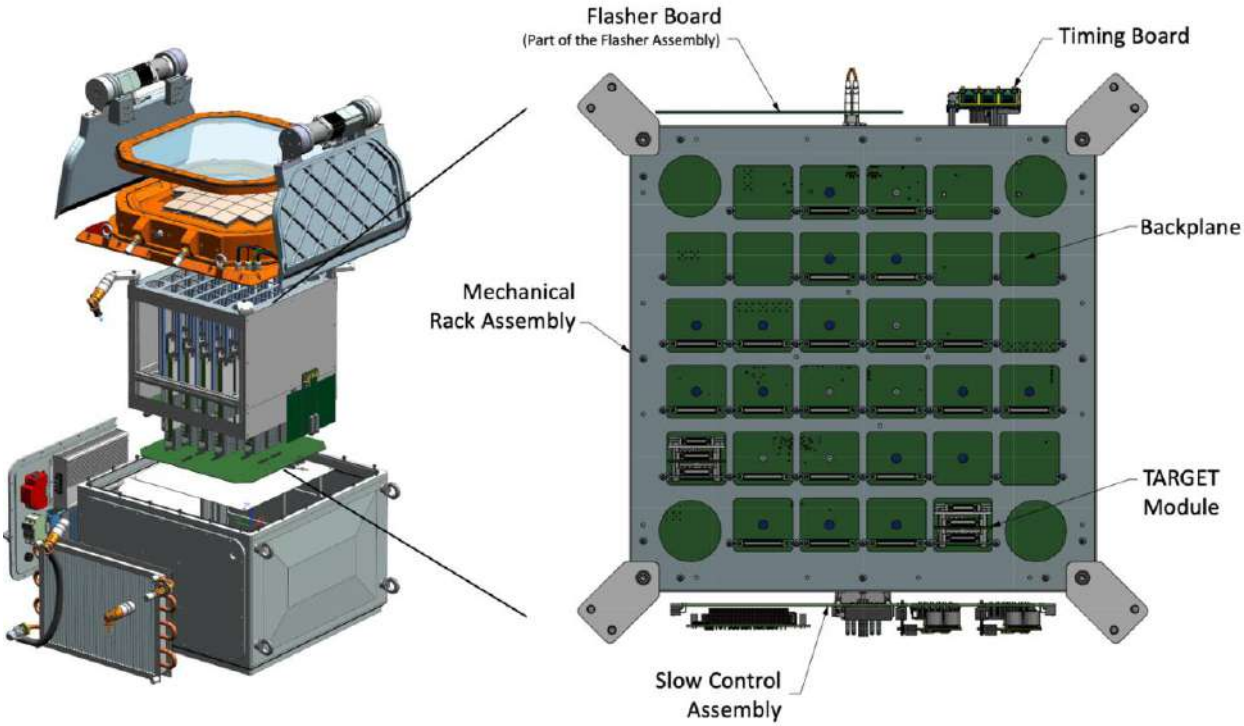
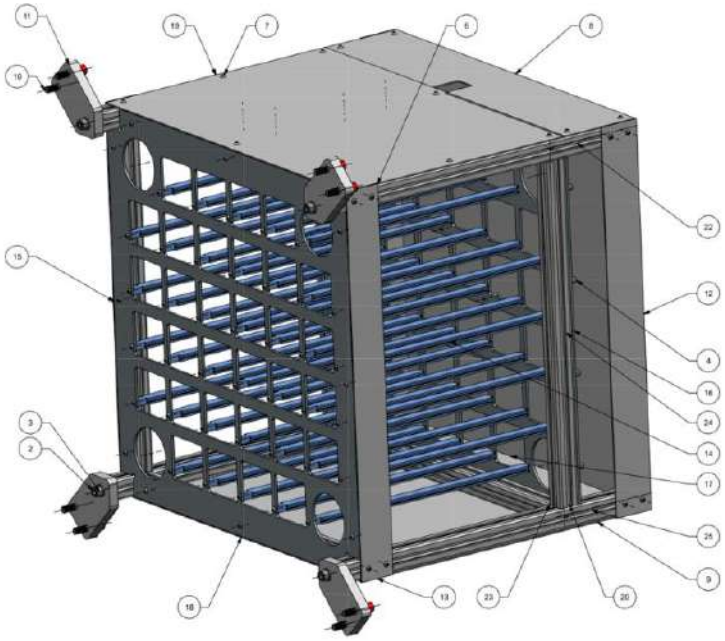


Figure 41: Electronics Rack Assembly, shown in context of the full Camera CAD. Note: not all TARGET Modules or connectors on the Backplane are shown.

7.4.1 Mechanical Rack Assembly

The Mechanical Rack Assembly (or simply 'rack' as shorthand) is a mechanical structure (see Figure 42) used to support the TARGET Modules, Backplane, Slow-Control Assembly, Timing Board, and Flasher Board. The rack frame is built with off-the-shelf extruded aluminium profiles, and has two panels with a pattern of square holes for the TARGET Modules at both ends. Unlike CHEC-S (and CHEC-M) all TARGET Modules are inserted to the rack, and mate to the Backplane in the same orientation. The Backplane is fixed to the back panel, and the top and bottom panels host the other boards.



PC NO	PART NAME
1	Backplane Guide Pin, T.E 223982-1
2	Hex Socket Head Cap Screw, ISO,M6x30
3	Plain Washer, ISO,6
4	SO-1015-03-02-02-N
5	Hex Socket Button Head Screw, ISO,M5x10
6	Hex Socket Button Head Screw, ISO,M3x8
7	Hex Socket Button Head Screw, ISO,M3x6
8	Top Panel 2
9	Bottom Panel 2
10	SSCA-M6-25-A48
11	Camera interface bracket
12	Backplane Air Baffle
13	Forward Air Baffle
14	SST TM Card Guide
15	TM Support Plate
16	TM-BP support plate
17	Rear Panel
18	Bottom Panel 1
19	Top Panel 1
20	MBS standard faster-5 (0.0.437.49)
21	MBS T-Slot_Nut_5_St_M3
22	MBS 20x20 Main Side Strut
23	MBS Main Top and Bottom Strut
24	MBS 20x20 Main Front and Rear Strut
25	Rack Frame Assy

Figure 42: The ERA Mechanical Rack.

7.4.2 Backplane PCA

The Backplane PCA ('Backplane', or BP for short) is a large board placed at the back of the rack. The SST Camera BP has major design changes with respect to the CHEC-S one (see Figure 43). Refer to [AD1] for a detailed overview of their motivations.

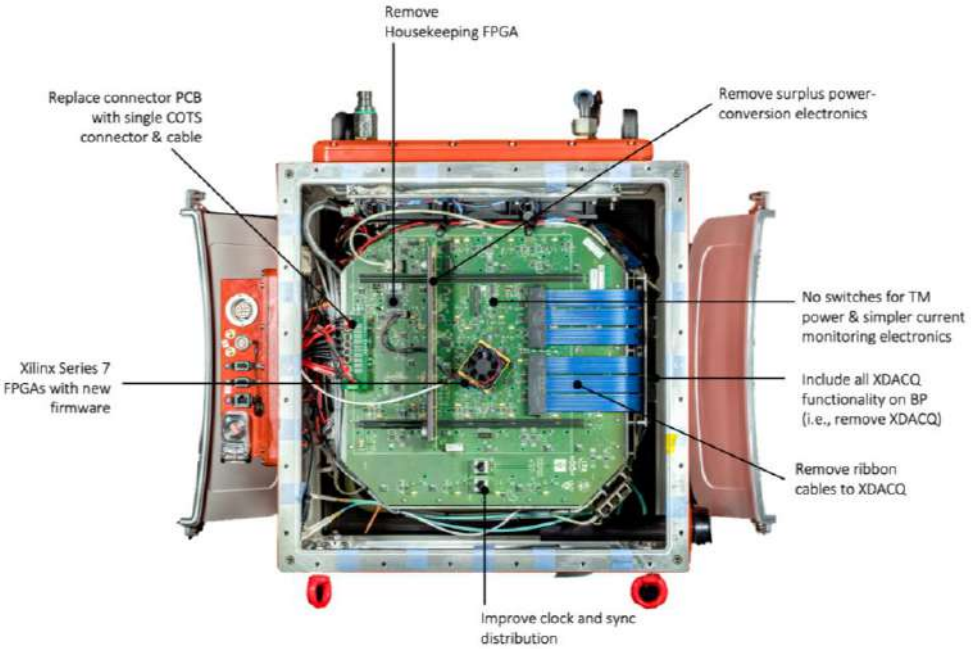


Figure 43: Picture of the CHEC-S from the back, illustrating some of the changes made to the Backplane.

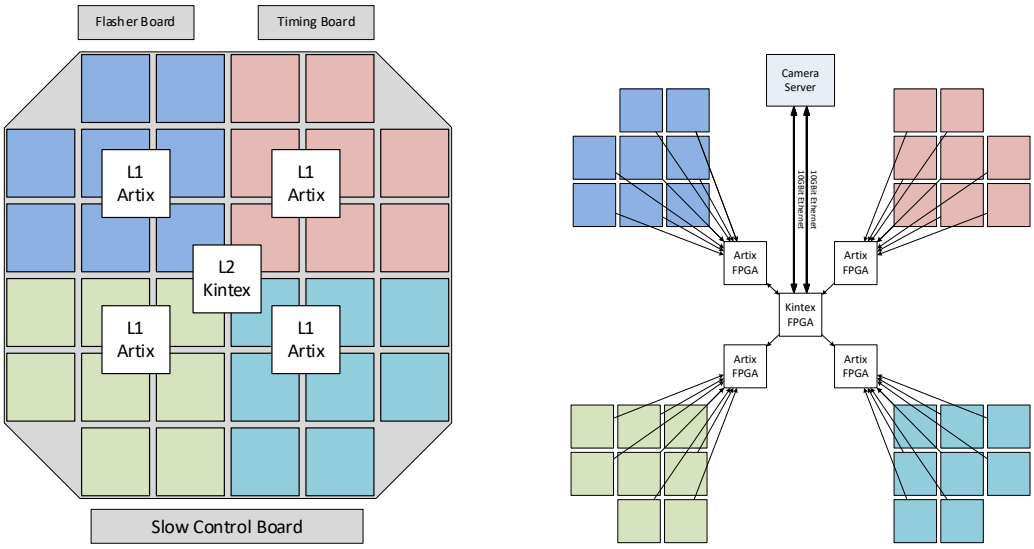


Figure 44: Left: Subdivision of the camera in four quadrants, corresponding to the four low-level backplane FPGAs. Right: The tree-like interconnection topology of the backplane.

The Backplane is a large board with five Xilinx Series 7 FPGAs on it: four Artix XC7A200T-3FFG1156C (A0, A1,A2,A3) and one Kintex KC7K325T-3FFG900C (K). The usage of multiple low-end and mid-tier Series 7 FPGAs instead of a single high-end Series 6 FPGA as in the CHEC-S backplane design reduces routing complexity, reduces power consumption, increases resource availability, improves timing performance and overall system stability. Moving away from the deprecated Series 6 improves parts availability, design longevity and maintainability. Furthermore, it allows the usage of the AXI/Aurora Chip2Chip FPGA interconnect, which reduces need for custom interfacing, and completely removes the need for the separate data aggregation board (i.e., XDACQ) used in CHEC-S.

The Backplane connects to 32 TARGET Modules (TMs). It is divided in four quadrants, with 8 TMs to per quadrant, all of which connected to one Artix FPGA; these are in turn connected to the central Kintex FPGA. Because of the hierarchy of the Trigger, the Artix FPGAs are also called “Level-1” FPGAs, whereas the central Kintex is the L2 FPGA. The Backplane is supported at the back-side of the Mechanical Rack that holds the TARGET Modules. The Timing, Flasher and Slow Control Boards are also attached to the sides of the same rack and are connected to the backplane. The Backplane is also connected to the Array Data Network (and from there to the Camera Server) via two redundant 10 Gbps Ethernet links over optical fibres.

The functionalities of the Backplane are the following:

- Formation of the Trigger from the SuperPixel signals
- Recording of the Trigger Pattern from the SuperPixel signals
- Distribution of the Readout signal to the Front-End (TARGET) Modules
- Distribution of the Clock and synchronization of the Front-End Modules with the Array Clock provided by the Timing Board.
- Trigger timing, both relative and absolute (using the Timing Board).
- Routing and Aggregation of Data and Slow Control Packets to/from the Front-End (TARGET) Modules
- Distribution, Control and Monitoring of main (24V) power and to the Front-End (TARGET) Modules
- Distribution of the Bias Voltage (48V) for the Front-End SiPMs

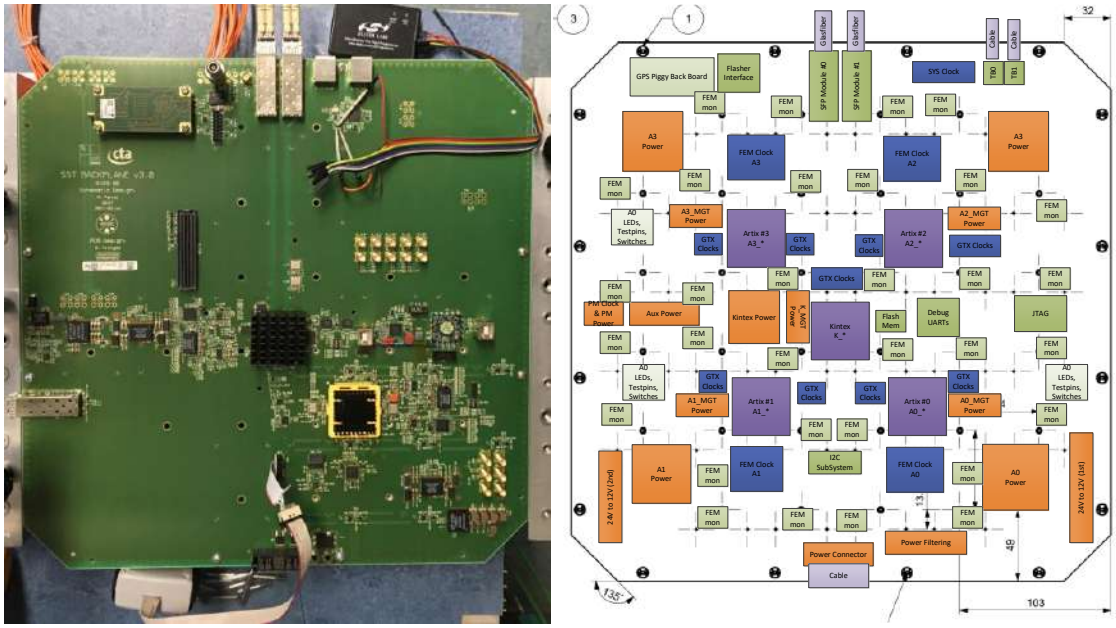


Figure 45: Backplane component placement.
Left: Prototype Quarter-backplane, with only one quadrant populated.
Right: Proposed component positioning on full-backplane

A description of how the Backplane functionality is implemented by means of the above-mentioned tree hierarchy follows.

7.4.2.1 Backplane Trigger Functionality

The trigger sources for the SST Camera are as follows:

- **Camera**: triggers when there is a time coincidence of any two neighbouring SuperPixels.
- **Internal**: triggers are internally generated by the Backplane. Trigger starting time, number of generated triggers and frequency are configurable.
- **External**: triggers on the rising edge of the "External Trigger" signal from the Timing Board.
- **Flasher**: triggers the camera at a fixed latency with respect to any of the signals sent to the Flasher Assembly.

The trigger source is identified with a flag and is stored at every event.

7.4.2.1.1 Camera Trigger

The Camera Trigger is designed to detect Cherenkov Air Showers by exploiting their coherence in time and space in order to distinguish them from background noise.
In the front-end, the analogue signal detected by the 2048 SiPM pixels at the camera focal plane is amplified, summed in groups of 4 pixels (the SuperPixels, SP), compared to a threshold and stretched to a certain length. Each Target Module produces 16 SuperPixels signals. These are routed to four L1 Artix FPGAs, one per quadrant. This results in a total of 512 asynchronous logic LVDS signals being transmitted from the TMs to the Backplane. The Camera Trigger must be generated whenever two neighbouring SuperPixels triggers are active at the same time.
The trigger generation functionality of the Backplane FPGA is distributed between the L1 and L2 FPGAs. In the L1 Artix FPGAs the incoming asynchronous SuperPixel signals are delayed with IODELAYs, then sampled at 1 GHz. Each SuperPixel can be individually enabled or disabled before getting to the coincidence logic. In order to trigger SuperPixel pairs crossing quadrant boundaries, the signals of the

23 SuperPixels situated along the inner quadrant edge are and forwarded to the central L2 Kintex FPGA via source-synchronous transmission.

The coincidence logic that determines the coincidences between neighbouring SuperPixels is based on a simple set of offsets *K*:

$$K = ((0,+1),(+1,+1),(+1,0),(+1,-1)).$$

So, if *P* is the group of pixel coordinates in a 2-dimensional space, the neighbouring pairs *N* are:

$$\forall p \in P, \forall k \in K \;\; N = (p, p+k)$$

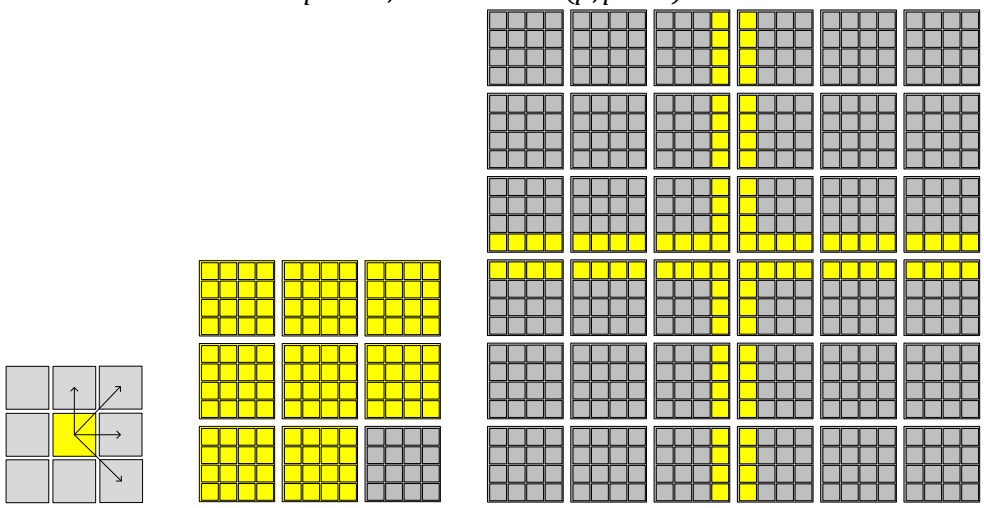


Figure 46: Backplane SuperPixel Coincidence Logic. From left to right: basic kernel, L1 logic space, L2 logic space. Pixels taking part to the coincidence are highlighted in yellow

P covers the full extent of the 2-dimensional space occupied by the SuperPixels. This algorithm can be used in the firmware to easily generate all required neighbouring pairs used for the determination of the coincidences. In the L1 case, the neighbours are within the Quadrant SuperPixels, so *P* is the Quadrant Space, 12x12; in the L2 case, the coincidences need to be established between Quadrant Edge SuperPixels, so *P* is the full Camera SuperPixel Space, 24x24.

Upon detecting the coincidence between two neighbouring SP trigger signals, the L1 FPGAs generate a trigger signal. These quadrant-level trigger signals are sent to the L2 FPGA, where they are delayed and their logical OR determines the camera-level trigger (the coincidences between the central four SP signals are handled directly by the L2 FPGA).

The camera-level trigger is timestamped with the internal relative timestamp, and is sent to the Timing Board for absolute timestamping. The trigger is optionally immediately propagated back to the TARGET Modules for synchronous data readout, or its relative timestamp is added to a queue for later asynchronous data readout. In the latter case, the relative timestamp of the trigger is sent to the modules via the AXI4Lite control bus.

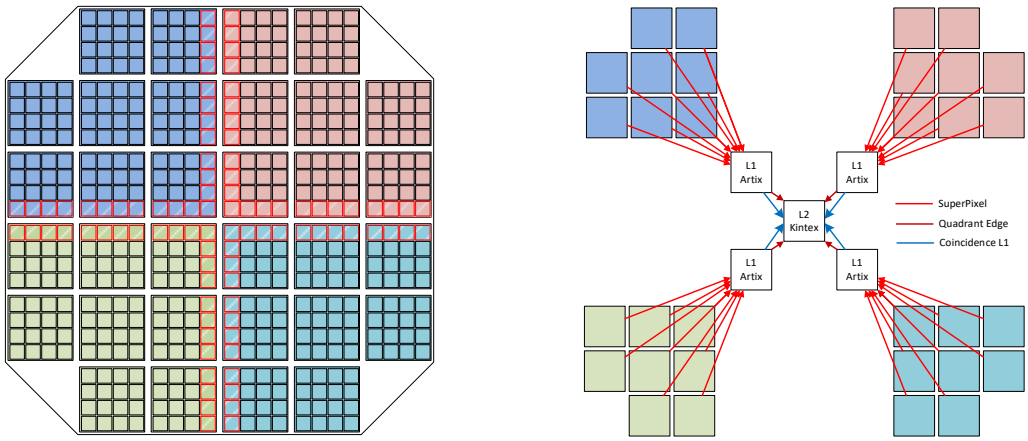


Figure 47: Left: Handling of superpixel triggers overlapping different camera quadrants. Right: Trigger interconnections present on the backplane.

7.4.2.1.2 Internal Trigger

The Backplane implements an internal trigger generator. This generator can issue any number (from 1 to infinity) of triggers to the camera with a settable frequency, and a settable starting time. It has an enable/disable port as well.

7.4.2.1.3 External Trigger

This trigger is generated by the EXTERNAL_TRIG signal of the Timing Board. In general, these can be either a single pulse (sent immediately or scheduled at a given time) or periodic trigger signals of a given frequency. Width of pulse is 16ns (or multiples thereof) and minimum period between pulses is 112 ns.

7.4.2.1.4 Flasher Trigger

The Flasher Unit calibration light pulses are emitted by four individual LED Flashers and carried to different locations via light fibres (see Figure 59):

- Under-the-lid calibration flasher – this flasher sends calibration light pulses travels through a scintillating fibre placed at the edge of the window. It provides the camera with an under-the-lid calibration and testing system.
- Corner flashers – these two flashers shoot light pulses from two of the camera Focal Plane Transition Plate corners, which illuminate the M2 mirror, and their reflection illuminates the camera focal plane.
- M2 centre flasher – this flasher shoots light pulses directly from the centre of the M2 mirror towards the camera focal plane. This light pulse is the most homogenous and is used for several calibration purposes, the most important of which is flat-fielding the camera.

When using the flasher, the camera may be triggered either by the SuperPixel Coincidence trigger due to the response to the flash of light itself, or by a delayed copy of the signal sent to the Flasher Board. This is necessary for the following use cases:

- the flashing light intensity is so low that self-triggering would be impractical (Single-Photoelectron)
- the timing of the pixels and SuperPixels input is to be calibrated vs. the system clock
- the flasher event needs to be tagged by a trigger flag.

To this end, the Backplane implements a trigger pulse generator, similar to the one used for the internal trigger, with the added functionalities of having two outputs: one with a controllable pulse width and the other with a settable delay. The non-delayed output P_1 is amplified by a buffer and its signal is sent

over coax cables to the Flasher Board, triggering the Flasher Assembly. The delayed output P_2 triggers the camera; it may be enabled or disabled, and its delay with respect to the non-delayed output is programmable from 0 to at least 16 us in steps of at least 8 ns. The jitter between P1 and P2 is very low.

7.4.2.2 Backplane Clock

The clock is generated by the timing board or alternatively by a local oscillator, distributed to all TM and FPGAs in the hierarchy, delay compensated and phase locked. The system clock uses Si534x chips with external feedback to maintain the phase coherence down to the TARGET Modules. The whole camera trigger and timestamping runs synchronously to it. Absolute time synchronization is implemented using a source-synchronous SYNC signal generated by the L2 FPGA and routed isochronously to the L1 FPGA and to all modules, along with its clock of 500 MHz. The time-critical READOUT signal is similarly source-synchronous with the same clock. The whole system is designed to work clock-synchronously with 1ns precision. The clock network and delay compensation scheme is illustrated in Figure 48.

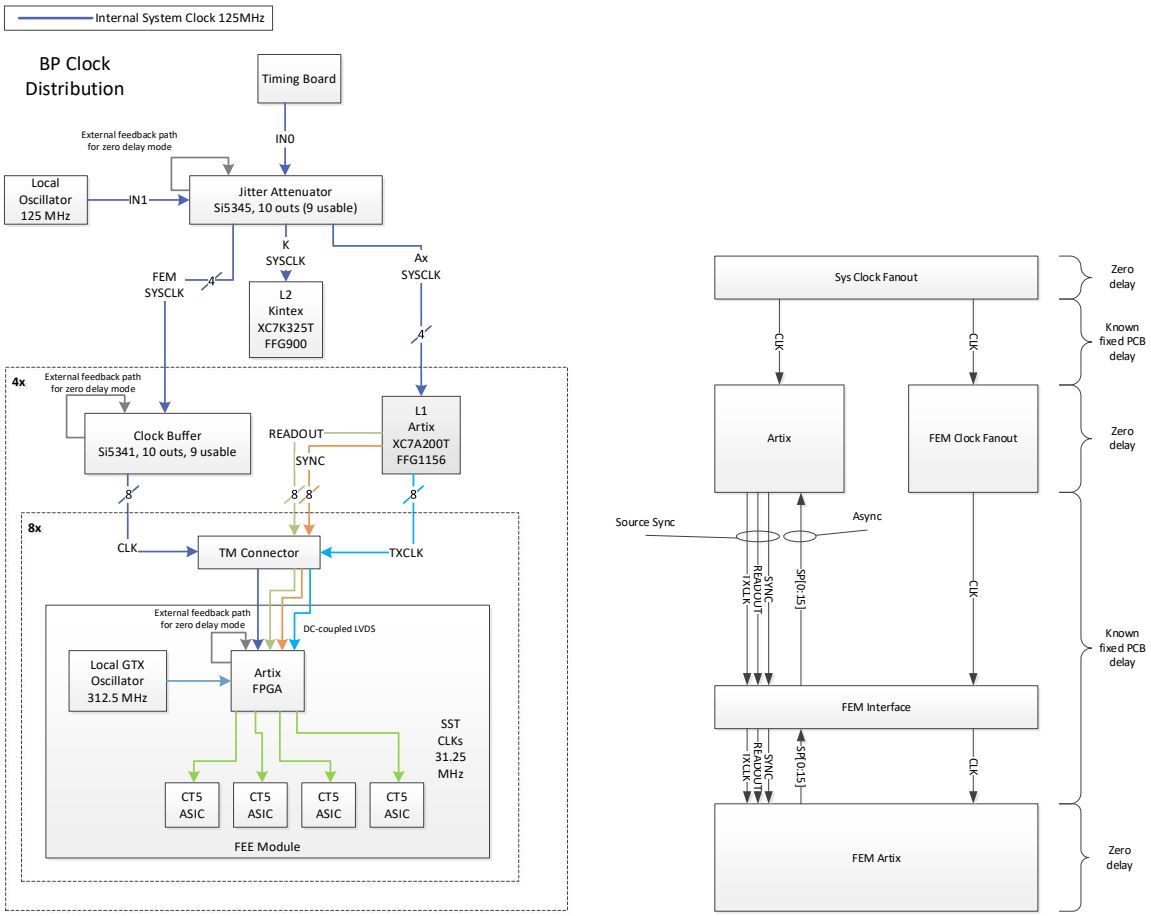


Figure 48: Proposed backplane clock network and phase compensation scheme

7.4.2.3 Backplane Readout

7.4.2.3.1 Readout and Busy

A “readout” trigger is any trigger (of any type/source), which will result in a readout of the camera.
A “busy” trigger is a trigger (of any type/source), which occurs while the camera is still busy reading out a previous event and that cannot be read out.

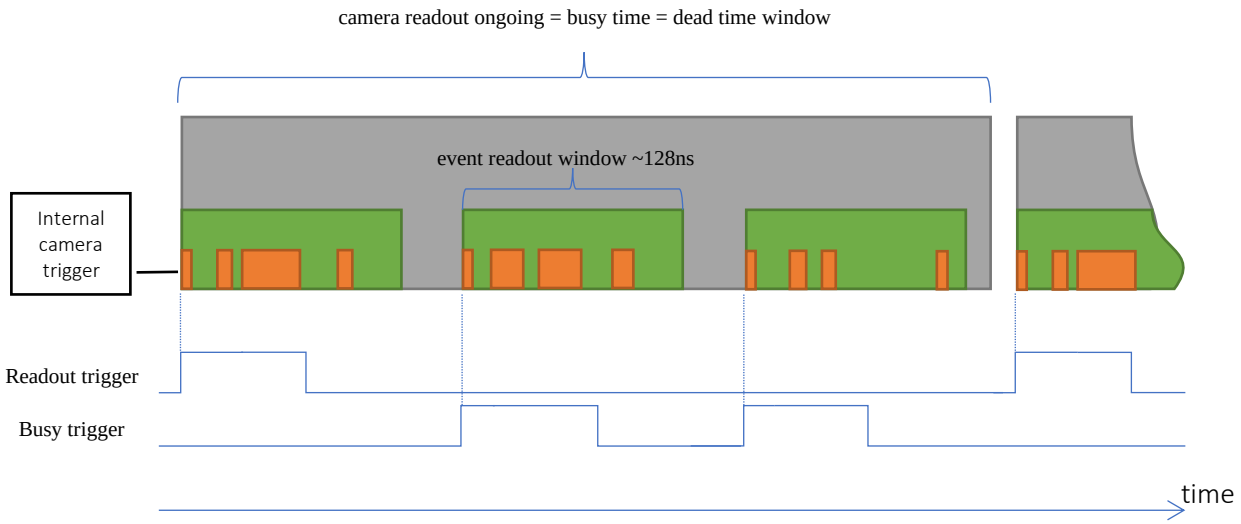


Figure 49 - Camera readout trigger example with several busy triggers

When the internal camera coincidence triggers on an air shower, it will be triggered by one of the first photons detected that belong to that air shower. Therefore, any additional camera coincidence trigger generated by the same air shower event after that first trigger should not be counted. A trigger is considered to belong to the same air shower event if it is within roughly 100 ns from the first trigger. This length in time corresponds to the event readout window, i.e. the time during which the signals from the SiPMs are digitized. The event readout window is a settable configuration parameter of the front-end modules and its default value is 128ns. It makes no sense to trigger the camera during that time, because a trigger for the event already happened and the data is being read. Therefore, no further trigger shall be issued during the event readout window.

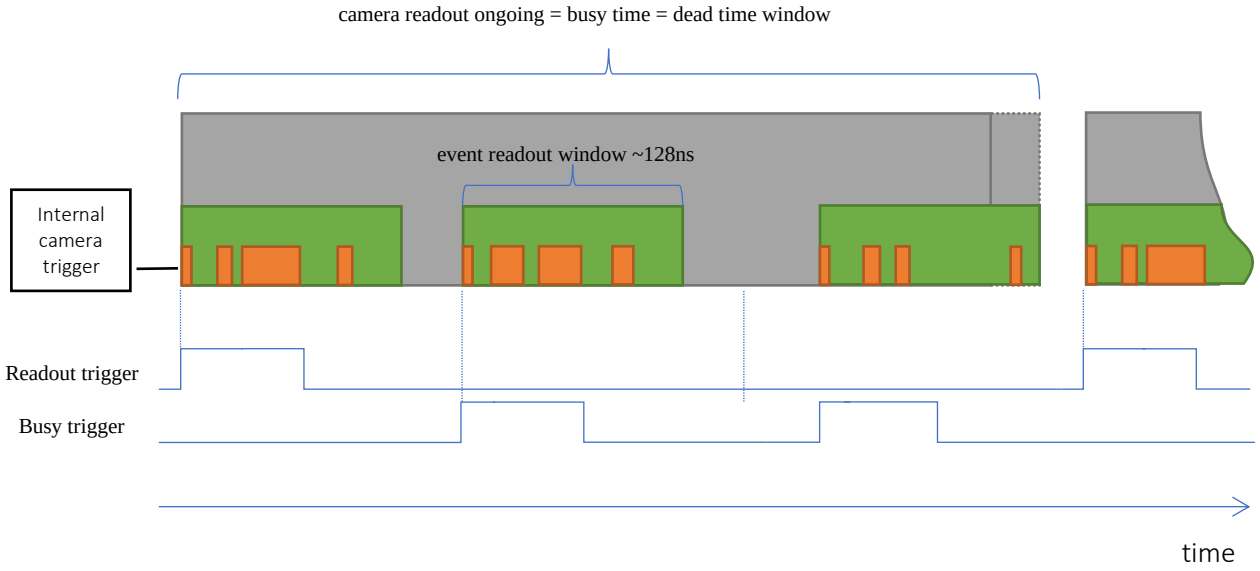


Figure 50 - Camera readout trigger example with a busy trigger readout-window that overlaps with the end of the deadtime window

7.4.2.3.2 Synchronous Readout

The process of reading out, sampling and storing the event data happening at the front-end-modules takes longer than 128ns. When it's started synchronously with a trigger, during that time the camera will busy, i.e., no further event may trigger a readout. The time during which the camera is busy with readout is called "dead-time window". Any camera trigger happening during the dead time window shall produce a "busy" trigger, and the camera shall record an event with all information except the (unavailable) event data (see Figure 49).

With this logic scheme, there is a chance that a (potential) air-shower event starts at the very end of the dead-time window, and its readout window spills over the "idle" time, with some coincidences potentially happening during it. This event shall create only a busy trigger, and the total camera dead-time window must be extended by the remaining readout-window time (see Figure 50).

7.4.2.3.3 Asynchronous Readout

The front-end modules sample signals continuously in a ring buffer, whose maximum depth is in of the past 16384 samples (i.e., 16384 ns), of which 4096 samples are used for in the SST. The TARGET Modules are capable of reading out any region of it asynchronously; in order to do so the backplane sends them a timestamp indicating the event starting time. This timestamp is a 64-bit counter incremented every ns, and it is called TACK for Time of Acquisition. In this readout mode, the dead-time is reduced considerably. The busy state due to pile-up of readout requests is avoided by pipelining them asynchronously.

In the CHEC-S implementation the TACK is broadcasted serially to all modules by the backplane via the READOUT signal. In the SST implementation, it is sent over the AXI4Lite Control line (see following section). In order for all of this to work, both backplane and TARGET Modules must keep a synchronous time counter, which is synchronized via the SYNC signal.

7.4.2.4 Backplane Slow Control Communication and Data Aggregation

The communication with Backplane and TARGET Modules is implemented using the Xilinx Aurora-AXI Bus infrastructure with a single point of access, the L2 FPGA (see Figure 44, right). The registers all FPGAs are mapped onto a single camera-wide address space which is efficiently accessible over a hierarchal AXI4Lite bus infrastructure, improving the efficiency of register and memory access dramatically with respect to the CHEC-S design. The data routing and aggregation now done by the XDACQ is accomplished with an AXIStream bus. Both busses are implemented on Aurora 8b10b links over LVDS lines between the FPGAs, using standard, off-the-shelf Xilinx Chip2Chip IP cores.

The 10 Gbps lines require special attention because of their tight impedance requirement. Because of this Rogers PCB material was used for the layers where they are laid out.

We tested the most critical links – the 6Gbps link between L1 and L2 FPGAs (Artix to Kintex) and the 10 Gbps one using a loopback via the two SFP optical fibre connectors. The results show that even in the worst-case scenario the eye-opening area is larger than 50% therefore the Bit Error Rate is expected to be very low (see Figure 51).

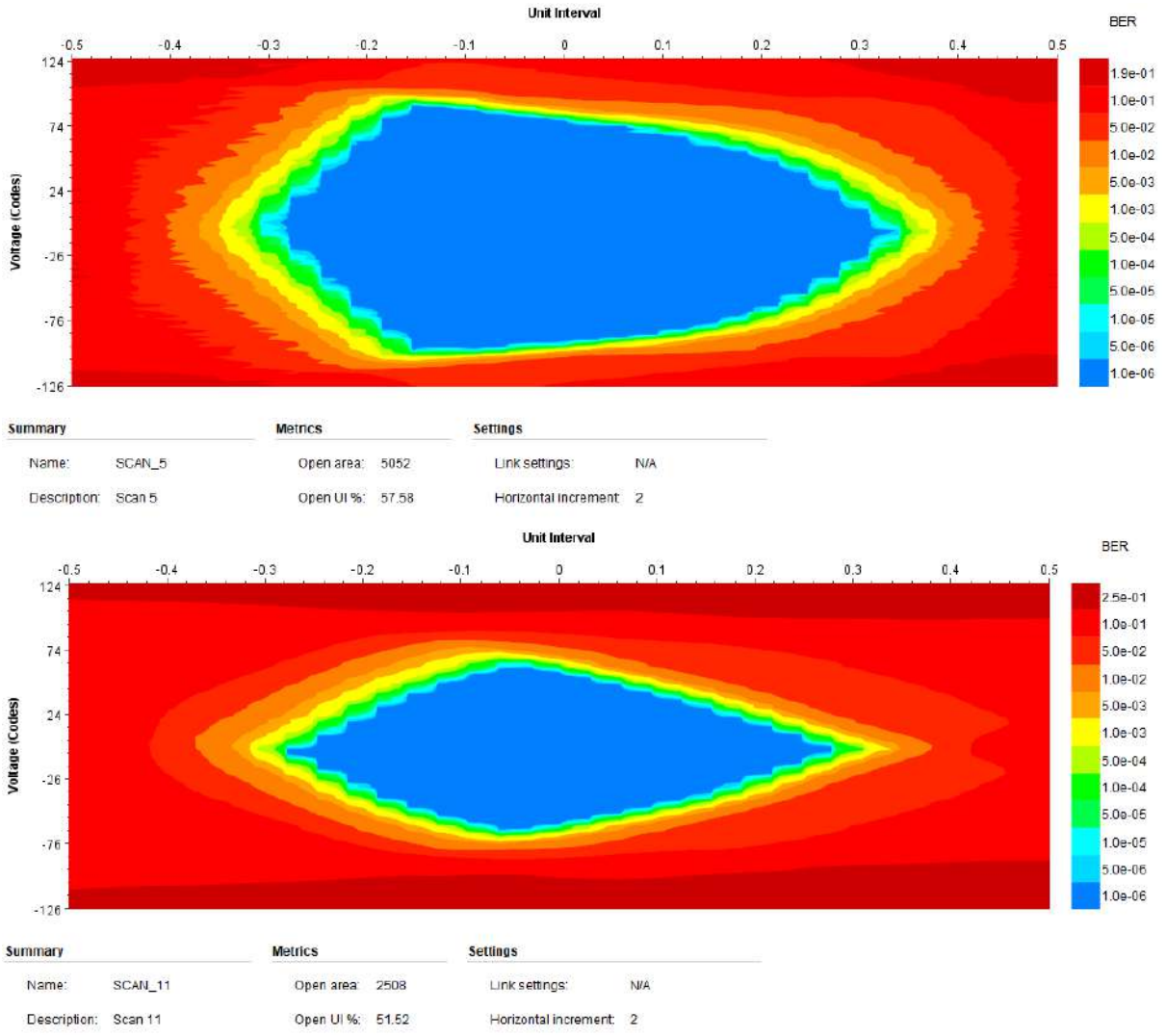


Figure 51: Worst-case eye diagrams of 6Gbps connection between L1 and L2 FPGAs (top) and 10Gbps connection (bottom, loopback between two L2 outputs)

7.4.2.5 Backplane Power Distribution

The power distribution concept is illustrated in Figure 52. The main power is used for all components with 24V. This reduces the current flow and eases the requirements for routing on the PCBs and the connectors.

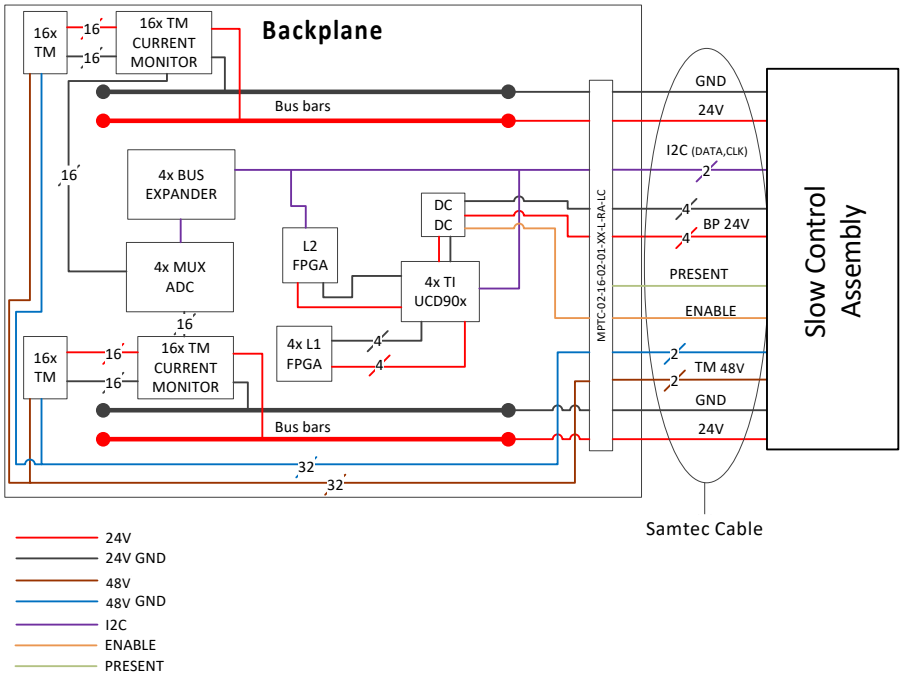


Figure 52: Power distribution and control concept.

All power is controlled and monitored by the Slow Control Subassembly via an I^2C bus, whose architecture is represented in Figure 53. The Kintex FPGA can also act as a bus master via a Bus Arbitrator Chip.

Devices on this bus include the power ICs of the L1 and L2 FPGAs, based on the LTM2974 and LTM4675 chips, the clock jitter attenuators and clock switching chips, the I/O expanders which check for the presence of the TM modules and switched them on or off using the enable signal of their main DC/DC converter, and the INA226A current monitors which measure the current and voltage of the TMs.

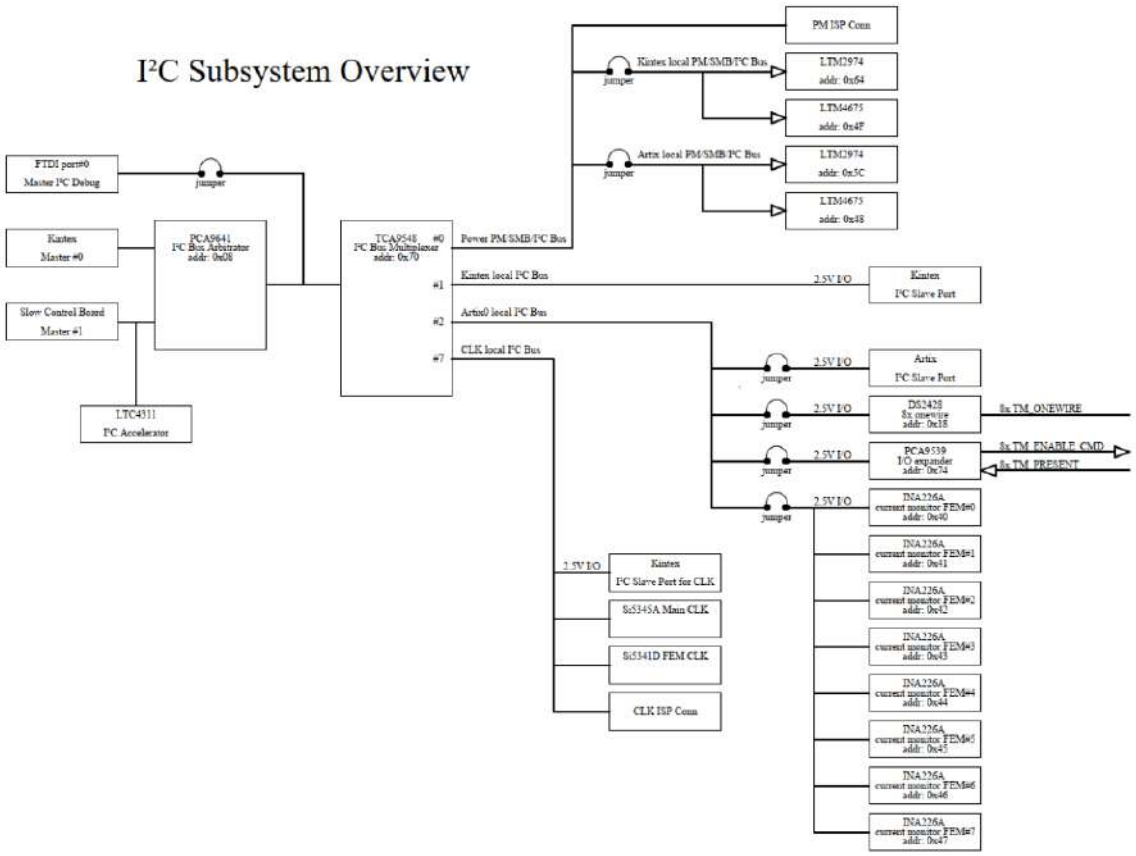


Figure 53: Backplane I2C Bus Network

In the CHEC-S architecture, the Backplane implemented discrete on-board switches to control the power delivery all TM modules and the slow control board had no direct control of it, thus that responsibility was shared between two sub-systems. In the new design, all power control and monitoring take place in a central place. The Backplane implements only the power distribution, and the power monitoring circuitry. The power to the target modules is switched and off using the enable signal of their main DC/DC converter.

7.4.3 Slow Control Subassembly

The Slow Control Subassembly (SCA) is responsible for power distribution, low-level control, instrument safety and housekeeping. It is composed of a motherboard (Slow Board PCA) with three mezzanines: the GECCO Board PCA and two Motor Driver PCAs (NP5A, NP5B) as shown in Figure 54.

The GECCO (Generic Ethernet-Chainable COntrol) Board (Figure 55) is the core of the SCA, it is a general-purpose board developed jointly with the MST FlashCAM. It features a 32-bit microcontroller and several I/O components, including ADCs for measuring analogue inputs, and support for 1x Ethernet SFP port and 2x Ethernet RJ45 100Mbps ports. The Slow Board hosts several I²C bus expanders and analogue mux chips and associated signal conditioning for expanding the range of the analogue inputs. It also includes the circuitry to control and monitor the power to all other subsystems of the Camera. The two Motor Driver Boards are commercial boards used to control the motors, their brakes and the encoders. Up to 6 temperature or relative humidity sensors may be connected (and positioned as desired around the camera). Communication with the SCA is via a single LC single-mode fibre.

The SCA firmware implements alerts and automatic reactions to prevent damage to the camera, and is capable of switching on/off all camera components except the Chiller (and does so automatically if communications to the CSW is lost for more than 60 seconds). The firmware can be remotely updated fibre the same fibre interface used for communications.

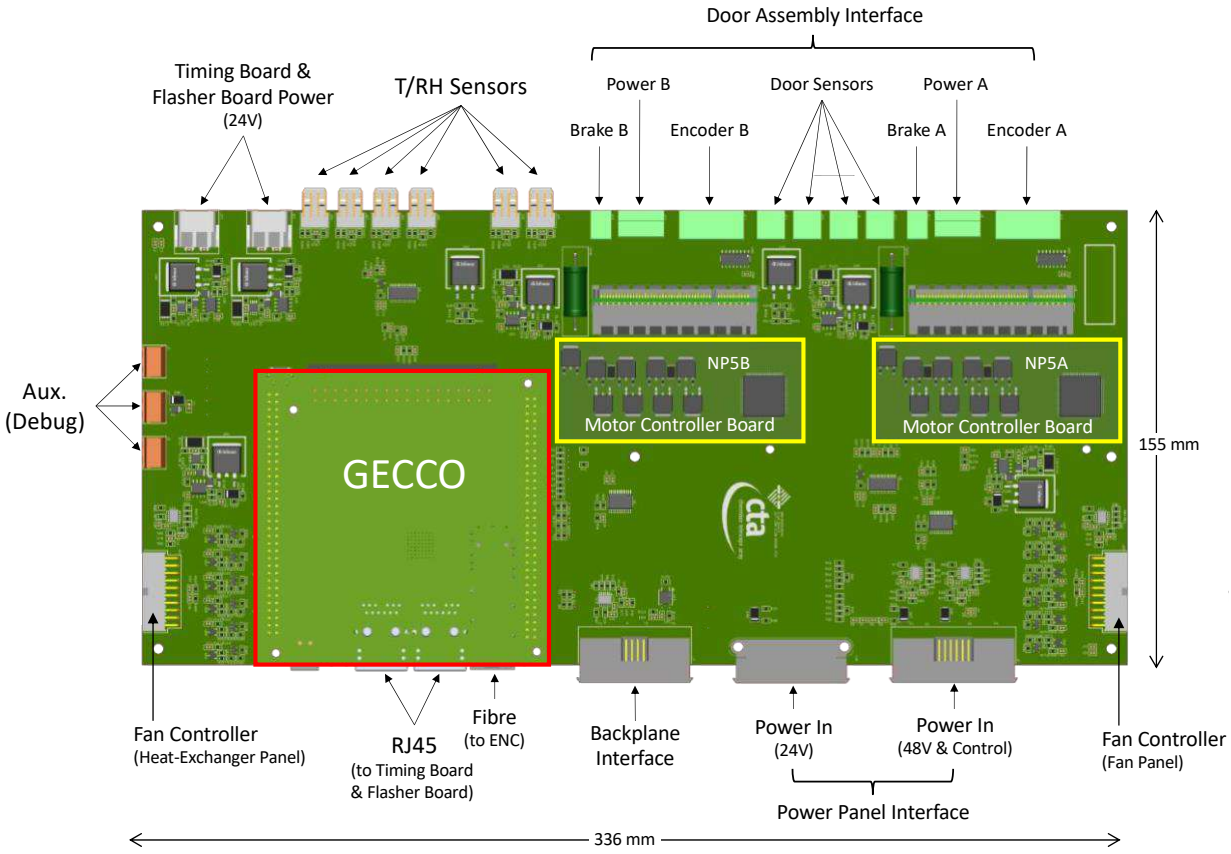


Figure 54: The Slow Control Assembly.

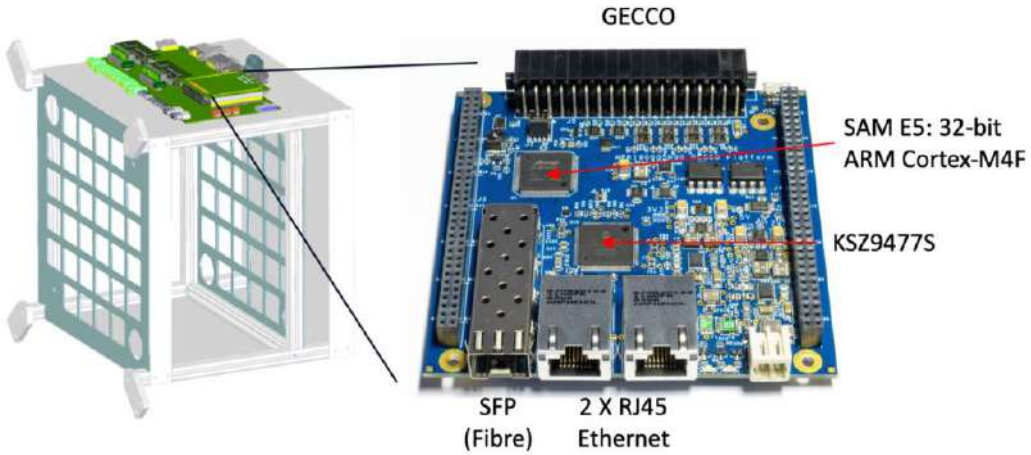


Figure 55: The SCA mounted on the ERA Rack, with a zoom of the GECCO board.

The interfaces to and from the SCA are outlined in Figure 56. The SCA provides the following functionality to the various camera elements:

Power Supplies. The main power supply (MeanWell UHP-1500-24PM) provides an auxiliary 12 V output that is always on. This is used to power the SCA. The SCA then provides the ability for both the main power supply (24V), and the high-voltage (48V) power supply to:

- enable and disable the output,
- monitor status optionally through SMBus / I2C (buffered),
- measure voltage and current.

The SCA routes the 24V and 48V lines to the Backplane, where 24V is used for power and both lines are fanned out and distributed to the TARGET Modules.

Backplane (& TARGET Modules). The connection between the SCA and the BP is via a single connector (labelled "BP Power" in Figure 54, see also Figure 52). The SCA can then:

- detect if the Backplane is connected,
- dontrol the BP Power via the BP DC/DC convertors,
- control and monitor TARGET Module power (voltage & current) a buffered I2C bus to the BP.

Fan Controllers (i.e., Heat-Exchanger Panel Assembly & Fan Panel Assembly). The SCA connects to the fan controllers in both ENC side panels via a single connector each, that provides:

- main power control for each fan tray (with ramping, overcurrent, monitoring),
- individual on/off for each fan,
- fan speed PWM setting and RPM monitoring through buffered I2C,
- temperature and relative humidity monitoring through buffered I2C.

Timing Board and Flasher Board. The SCA contains two generic "Power Units" that supply 24V to the Timing Board and Flasher Board. Each connection provides: power, control of the power (including ramping), overcurrent protection, and voltage & current monitoring. The GECCO implements a 3-port switch, two of which support Ethernet RJ45 100Mbps ports, and are connected to the Timing Board and Flasher Board for control and monitoring.

Door Assembly. The SCA provides control of the camera Door Assembly via the two on-board Motor Controller Boards (Nanotec NP5-4). These boards interfaces to the GECCO via a simple set of control lines to command the Door Assembly to open/close and monitor the status (an SPI interface is also provided to remotely update the firmware on the motor controllers). The Motor Controller Board firmware provides the main power control for each door motor (with ramping, overcurrent protection and monitoring of encoder position). A Ballast circuit for the motors is provided on the Slow Board to protect other elements of the camera against reverse currents from the motors, and is configured in Motor Controller Board firmware. The Door Assembly position sensors are routed to both Motor Controller Boards and the GECCO and are used to determine the door status.

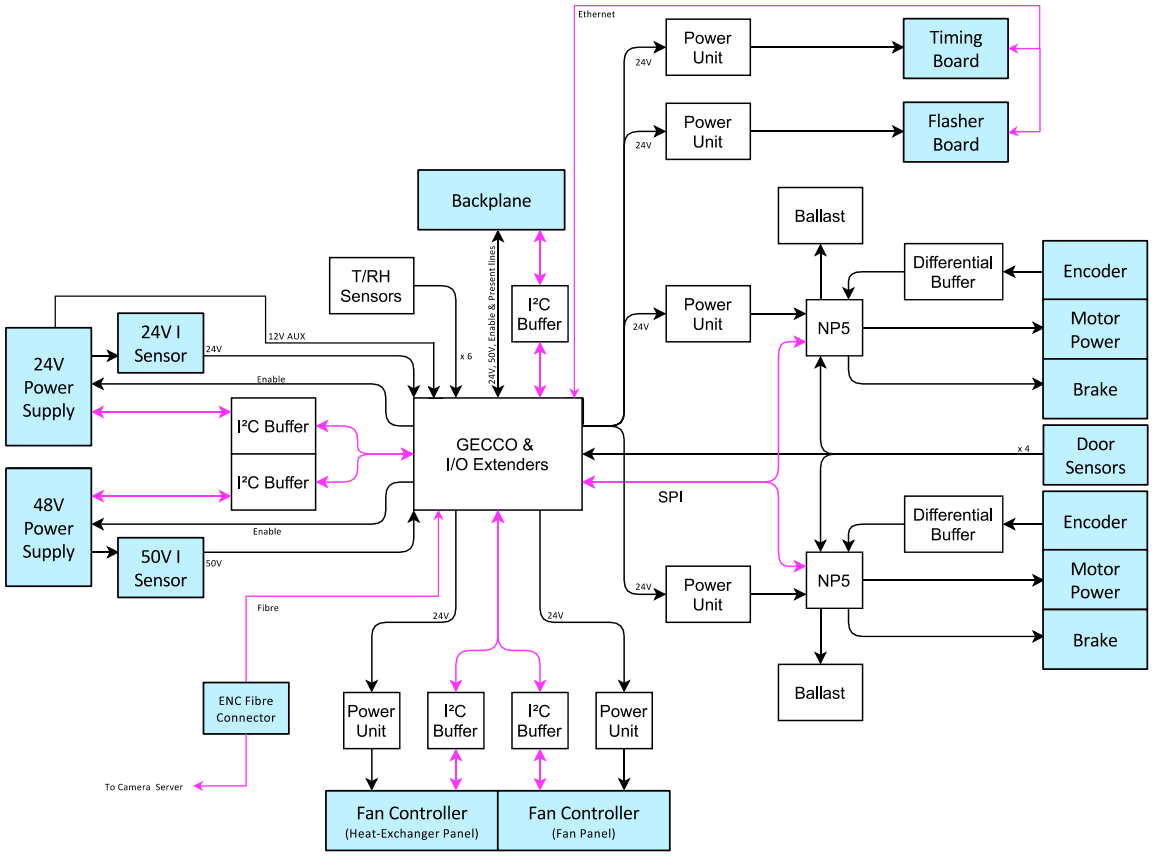


Figure 56: Schematic view of the interfaces and functions of the SCA. Magenta indicates communications. Blue boxes indicate elements external to the SCA.

7.4.4 ERA Cabling and Connectors

The ERA includes several internal cables, and cables that form the power and communication interface between the active camera elements and the power supplies and connectors mounted on the ENC. Note: motor cables are part of the FPA.

- **ERA – to – ENC Fibre:** All communication to the camera is via a single 12-core fibre, internally this is routed between the ENC and ERA using a single 12-core MTP to LC fibre fanout cable, customised such that only used fibres are present and have custom pig-tail lengths. On the ENC side, the MTP connector mates to the Neutrik MTP fibre-bulk-head connector (see Section 7.1). On the ERA side, one fibre connects to the SFP connector on the SCA, one to the Timing Board, and two to the Backplane (for 10 Gbps links, one of which is a backup) (Figure 57).
- **ERA – to ENC Power:** Power is input to the ERA from the ENC Power Panel Assembly via two cables, one carrying 24V, and the other carrying 48V and control and monitoring for the power supplies. 24V Cable: Samtec MPSS-06-14-L-XX.XX-SR. 48V+Control Cable: MPCC-2-24-2-L-44-XX.XX-S.
- **SCA – Backplane:** Connection from the SCA to provide power to the BP and TM, including control and monitoring signals. Cable: Samtec MPCC-2-16-2-L-44-XX.XX-D-NUS (Figure 57).
- **SCA – Fan Controllers:** Provides power and control to the fans. Identical pinouts. Power for each fan can be switched independently. Cable: Samtec MMSD-10-20-L-XX.XX-D-K-LDX.
- **SCA – Timing Board:** Power via TE connectivity MATE-N-LOK 5.08 plug (1-480318-0). Ethernet via CAT6 cable.

- **SCA – Flasher Board:** As for the SCA-Timing Board cables.
- **SCA – Sensors:** Up to six cables connecting T or RH sensors to the SCA. Cable: Molex 2.50mm Pitch Mini-Latch Receptacle Housing (511910400).
- **Backplane – Flasher Board:** SMA providing a trigger input to the Flasher from the Backplane.

Figure 57: Example ERA cables, showing the ERA-to-Backplane cable and the ERA-to-ENC fibre.

7.4.5 Timing Board

The baseline choice of timing solution for the SST Camera is to use a dedicated Timing Board identical to that used in CHEC-S: the SevenSolutions ZEN-CTA board based on the Xilinx Zynq XC7Z015-1CLG485C FPGA (see Figure 58). This White Rabbit hardware is procured commercially, however, the White Rabbit protocol is a de-facto industry standard and its reference implementation firmware IP is open source. This opens up the alternative option of implementing the Timing Board functionality directly on the Backplane L2 FPGA, foregoing the need of a dedicated board inside the camera. This option is under investigation.

The Timing Board provides a clock to the Backplane, along with a 1 PPS signal. The Backplane may then provide absolute timestamps to every event. Alternatively, an asynchronous trigger pulse may be sent to the Timing Board from the Backplane, which can then create an absolute time stamp. An event counter is kept in sync between the Timing Board and the Backplane. Control and monitoring of the Timing Board is via the Ethernet Management Port, connected to the Slow Control Assembly, and then in-turn accessible via the Camera slow control network.

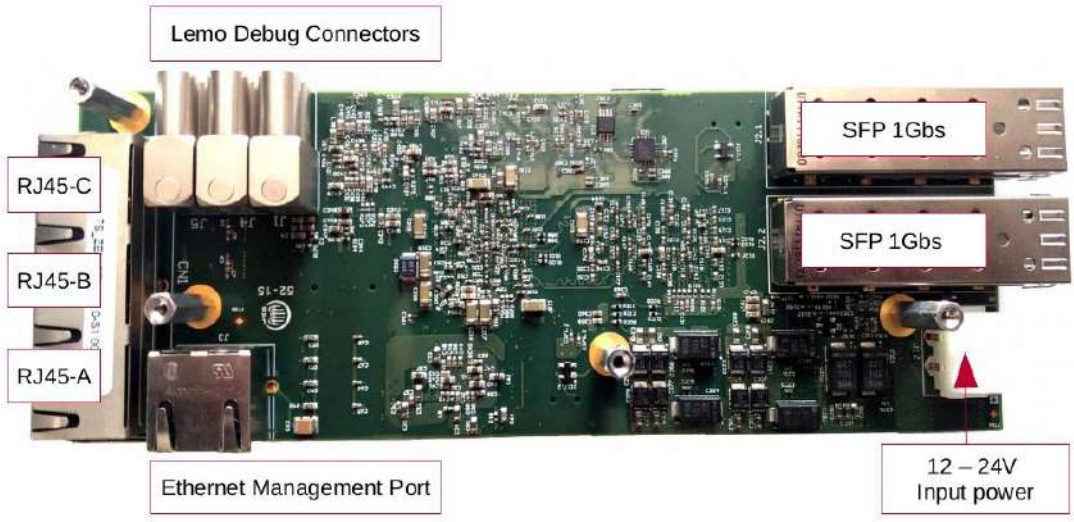


Figure 58: Picture of a Seven Solutions ZEN-CTA Timing Board

7.5 Flasher Assembly

The Flasher Assembly (or Flasher for short) (Table 9) is mounted to the top of the mechanical rack (next to the Timing Board) and consists of a mother board hosting a GECCO and four daughter boards, each with a fast-pulsed LED fibre coupled to the rest of the camera, providing an internal illumination source for calibrating the camera. The GECCO provides control and monitoring as per the SCA. The daughter boards each contain a driver circuit that allows an on-board LED to be pulsed over ~3 orders of magnitude with pulse durations of ~2 ns. The mother board contains programmable delay chips to control the exact time of LED pulsing individually for each daughter board in 250 ps steps following a trigger pulse input from the Backplane via SMA. The LEDs all fibre coupled and routed around the camera as shown in Figure 59. One fibre runs to a scintillating fibre in the focal plane, that is routed around the inside of the window glass to provide a non-uniform source of illumination with the doors closed. Two LEDs are fibre coupled to diffusers in the focal plane corners, titled to illuminate the camera focal plane via reflection from M2 mirror when installed on the telescope. The fourth LED is fibre coupled to a bulk-head connector on the ENC, which is used to connect another fibre to the rear of the M2, where the light is again diffused and illuminates the camera directly via a hole in the centre of the M2 (see Section 7.6.3 for further details of the External Illumination Assembly). Figure 60 shows the currently envisaged geometry of the Flasher Mother Board, and Figure 61 shows a schematic view of the Flasher Assembly.

Table 9: Flasher Assembly PBS

PBS Code	PBS Item	Description
SST.4.1.5.1	Flasher Mother Board	Large PCA housing the GECCO and four Flasher Daughter Boards.
SST.4.1.5.2	Flasher Daughter Board	Small PCA housing an LED and driver circuit.
SST.4.1.5.3	GECCO	As per the SCA.
SST.4.1.5.4	Fittings and Fixtures	All items needed to secure and interface the LED flashers to the rest of the camera, including optics for illuminating the M2 from the corners of the camera.
SST.4.1.5.5	Internal Fibre Cabling	Optical fibre cables running from the LEDs on the Flasher to connection points in the ENC and FPA.
SST.4.1.5.6	Flasher Firmware	The firmware for the LED flashers, integrated into the GECCO.

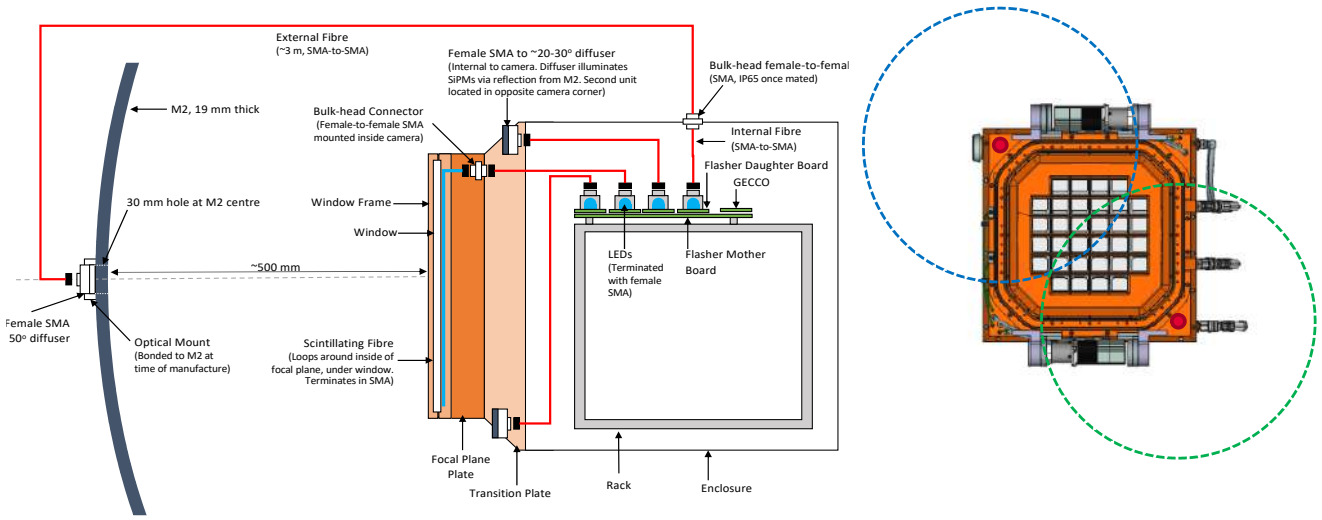


Figure 59: Cartoon of the Flasher Assembly and External Illumination Assembly geometry. Not to scale.

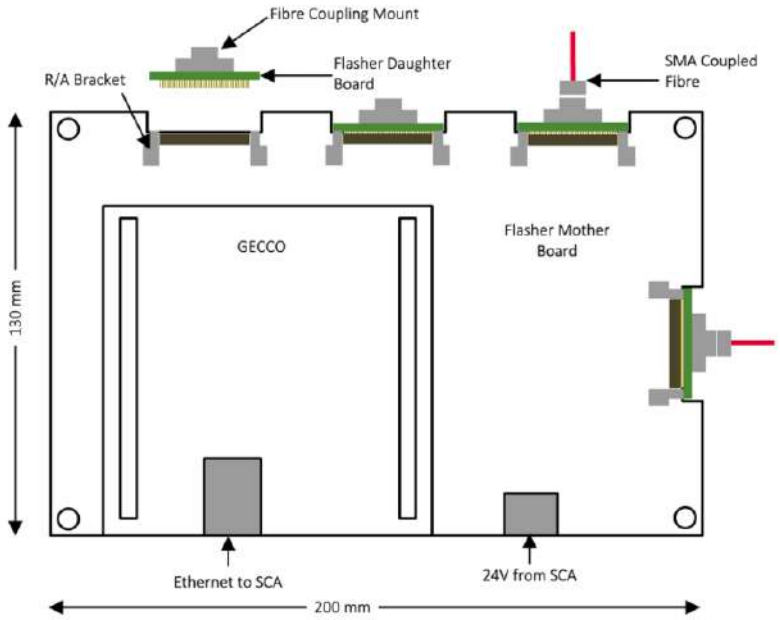


Figure 60: Currently envisaged geometry of the Flasher Mother Board.

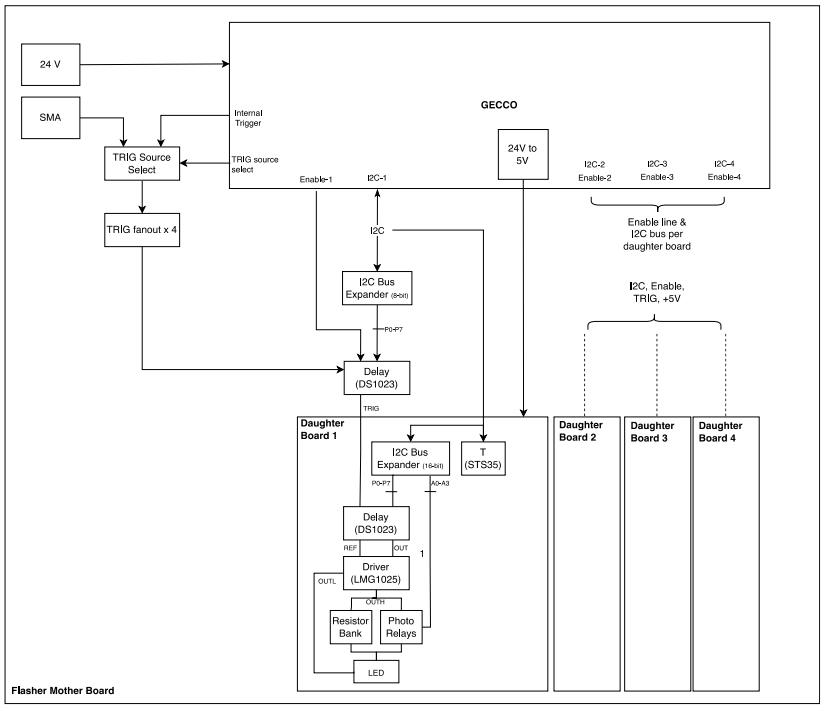


Figure 61: Schematic view of the Flasher Assembly.

The Flasher Daughter Board uses a single Bivar UV3TZ-400-15 UV LED. The LED is driven by the LMG1025 chip from Texas Instruments. Designed for automotive LIDAR applications, this gate driver has typical rise and fall times of 650ps and 850ps and can produce 5V pulse widths as short as 1.25ns. The LMG1025 is designed to drive a GaN FET to switch a LIDAR source, but with pull-up and pull-down current limits of 7A and 5A it can drive a standard or high-brightness LED directly. In order to control the intensity of the driving pulse, five resistors, connected in series, are placed between the LMG1025 output and the LED anode. The resistors are shorted out by TLP3475 photo-relays which provide fast response times. A Maxim Integrated DS1023S-25+ programmable timing element is used to generate a

digitally-programmable pulse of variable width, from essentially zero (+/-0.125ns) to a maximum of 62.5ns. This pulse triggers the LMG1025. By combining the pulse width of the DS1023S-25+ output and the 16 possible photorelay combinations, many brightness levels from ~1 p.e. to ~1000 p.e. per camera pixel can be covered. The daughter board also includes an I2C temperature sensor mounted close to the LED (and thermally couple via the fibre-mount), that also provides a unique serial number to every board. An I2C port expander provides control of the photorelays and DS1023S-25+. See Figure 62 for the LED driver circuit.

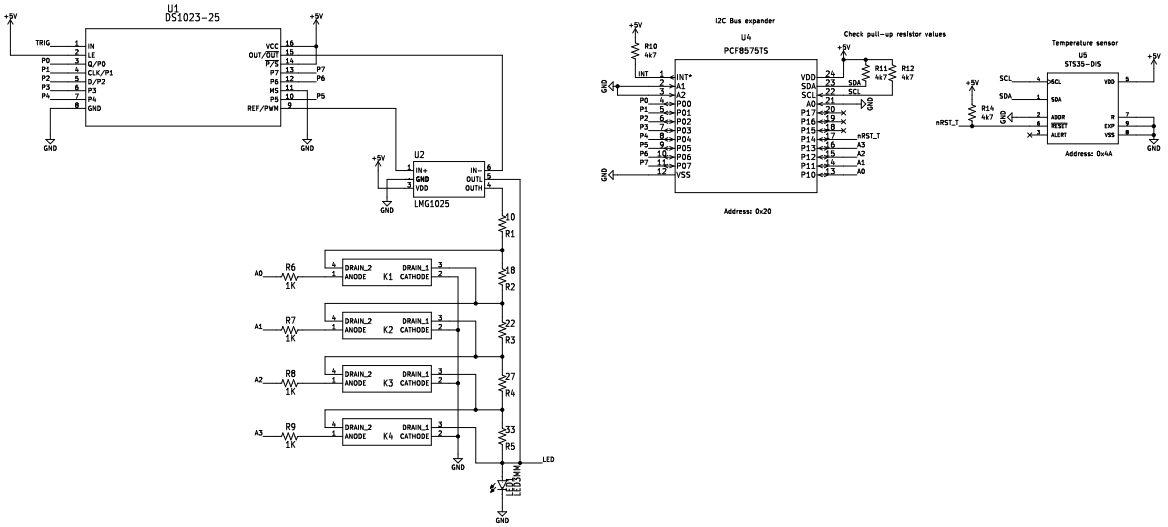


Figure 62: LED Flasher Board circuit diagram.

The Flasher Assembly is an evolution of the CHEC flasher-v3 units. See Figure 63 for a picture of the flasher-v3, and a CAD image of the current Flasher Daughter Board design. The driver circuit and choice of LED remain unchanged, and all changes are to do with integrating multiple LEDs into the camera in an efficient way.

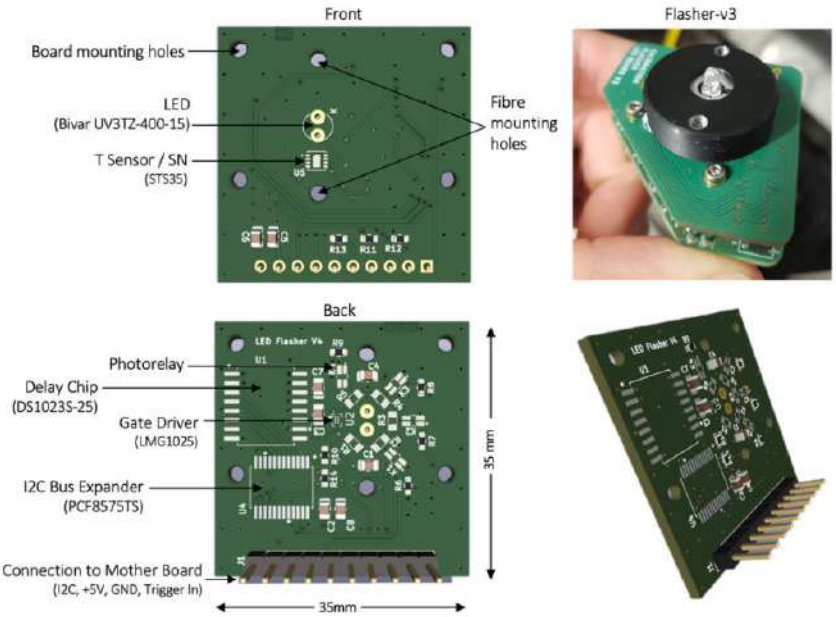


Figure 63: CAD images of the Flasher Daughter Board (also known as the Flasher-v4), with a photo of the existing Flasher-v3 for comparison.

7.6 Camera Support Systems (CSS)

The Camera Support Systems consist of items located at, or installed on, the telescope that are not part of the Camera Unit. As listed in Table 10, the CSS consist of: the Chiller Assembly, the External Cabling and the External Illumination Assembly.

Table 10: Camera Support Systems PBS.

PBS Code	PBS Item	Description
SST.4.2.1	**Chiller Assembly**	The camera chiller, heater and associated pipe work.
SST.4.2.1.1	Chiller	The camera chiller as purchased from the manufacturer.
SST.4.2.1.2	Pipework	All connectors and pipework associated with the camera chiller and heater loop external to the CU.
SST.4.2.2	**External Cabling**	All cabling external to the CU and attached to the CU and routed via the Telescope Structure.
SST.4.2.2.1	External Fibre Cabling	A single multi-core cable connected between the CU and the Telescope Structure Network cabinet.
SST.4.2.2.2	External Power Cabling	The cable carrying 240 V to the CU from the Telescope Structure Power cabinet.
SST.4.2.3	**External Illumination Assembly**	The external illumination fibre, routed to M2 and coupled to an optical system to illuminate the camera.
SST.4.2.3.1	External Illumination Fibre	Optical fibre.
SST.4.2.3.2	M2 Illumination Assembly	Nominally a small housing and engineered diffuser.

7.6.1 Chiller Assembly

The Chiller Assembly consists of the chiller coupled to the Camera Unit via a set of pipework. Two chillers with similar performance were evaluated for CHEC-S, the Rittal SK3336.209 and the Lauda Ultracool UC4, both rated for external operation with add-ons for extreme conditions. Neither were found to offer the temperature stability, functionality, or remote interfaces ideal for the SST. Following specification of the chiller functionality and performance, a request was made to several companies and two further candidates were identified with roughly equivalent parameters from Thermex Solutions and Laser Chill, as listed in Table 11. Both are suitable for outdoor use without a shelter.

Table 11: Chiller properties.

Parameter	Spec.	Thermex Solutions	Laser Chill
Operating voltage	230V / 50Hz	220-240V / 50Hz	220-240V / 50Hz
Cooling capacity	at least 1.5 kW	3 kW	2.15 kW
Heating power	Must Heat	2 kW	1 kW
Rated operating altitude	2100 m ASL	2000 m ASL	TBD
Operating ambient temperature range	[-15, +35]	[-20, +35]	[-20, +48]
Survival ambient temperature range	[-15, +35]	[-20, +90]	[-20, +48]
Settable T Range	At least [+8, +12]	[+5, +15]	[+4, +12]
Temperature Stability	< ±0.4°C	±0.2°C	±0.2°C
Flow rate	>10 l/min	54 l/min	10 - 20 l/min
Delivery Pressure	3 - 6 bar	3 bar	2.9 - 5 bar
Tank capacity	>20L	75 l	20 l
Weight (unfilled)	110 kg	180 kg	107 kg
Foot print (mm x mm)	<1m x <1m	683 x 1103	800 x 800
Height (mm)	<2m	1090	800
Protection level	IP54	IP55	IP55
Pipe connections	3/4" or 1" FBSP	1" FBSP	1" FBSP
Remote on/off	Required	Yes	Yes
Control connection	RJ45	RJ45	RJ45
Control interface	TCP or UDP	Modbus TCP/IP	Modbus TCP/IP

Critically, compared to the Rittal and Lauda units, the Thermex Solutions and Laser Chill units can heat as well as cool and offer better temperature stability. Heating will be used to maintain a manageable

temperature inside the Camera Unit during extreme conditions onsite. Temperature stability is important, as the gain of the SiPMs is temperature dependent.

The SiPM power consumption is explained in Section 7.2.4.3. The remainder of the heat dissipation in the camera from components is dominated by the Target Modules, fans and the Backplane. The doors system and heaters also require significant power, but the doors will not require power continuously and the heaters will only be required to keep the camera warm if all Target Modules are off. A maximum of ~950 W power consumption is expected by the camera under normal observing conditions. In extreme bright conditions this could increase to ~1.25 kW due to the increased current draw of the SiPMs and amplifiers. When moving, the doors create an additional 200-400 W (depending on speed, and if both are operated simultaneously), but this is not essential to consider for cooling concerns. Taking into account a safety margin, and ensuring passive safety in the event of failure of active bias control, we choose chiller models with a cooling capacity of at least 1.5 kW, and power supplies adequate to allow the doors to be closed even under extreme illumination with all electronics and SiPMs enabled.

The chiller will be placed on the ground close to the telescope structure, clearing the radius of movement. Due to the chiller size and weight, it cannot be placed on the telescope structure, nor inside the telescope tower. Placement on the ground greatly simplifies installation and maintenance.

The temperature of the refrigerant is controllable for both chiller candidate and the maximum cooling power is above the 1.25 kW required to cool the camera. The nominal refrigerant temperature will be set to 8-10°C but can be varied in a wider range depending on ambient conditions. The refrigerant liquid will be carried by a hose winding through the telescope structure; tests on the ASTRI prototype showed that the required hose length does not hinder the cooling capacity of the system. All connections on the pipework running from the chiller to the Camera Unit will be made with the same Staubli quick-release connectors as used on the Camera Unit itself (see Section 7.1.4).

7.6.2 External Cabling

Only two external cables are required. A power cable, and a fibre optic cable. The 3-core power cable carries mains, 230 V / 50 Hz from the telescope power cabinet (located at the back of the M1 mirror) to the camera. The power cable terminates in the cabinet with a circuit breaker. At the camera end, a Fischer WSO 104 Z040-80+ right-angle plug terminates the cable (see Figure 14). The fibre cable is a 12-core Neutrik opticalCON Lite single-mode cable (NKO12SA-L-0-15), which terminates with IP65-rated MPO (MTP) connectors at each end (Figure 64). At the camera end, the cable mates to the Neutrik NO12FDW-A chassis connector. The cable is routed to a passive interface at the base of the telescope tower and patch to CTAO fibres. The fibres within the cable are single mode, G.657A2, chosen for the tight minimum bend radius of 10 mm, and compatible with the CTAO standard fibre choice of G.652.

Figure 64: Neutrik NKO12SA-L-0-15, opticalCON Lite single-mode cable.

7.6.3 External Illumination Assembly (EIA)

The External Illumination Assembly (EIA) extends the Flasher Assembly (Section 7.5) from the Camera Unit to the back of the M2 mirror to provide a controllable and well-understood pulsed illumination level at the camera focal plane (see Figure 59 for a schematic of the LED Flasher Assembly and the EIA).

The EIA consists of a fibre-optic cable and some mechanics at the rear of M2 (see Figure 65). The fibre-cable, is a ruggedised, ~3 m, 1500 µm core fibre, coupled to the Camera Unit via an SMA-to-SMA bulk-head connector.

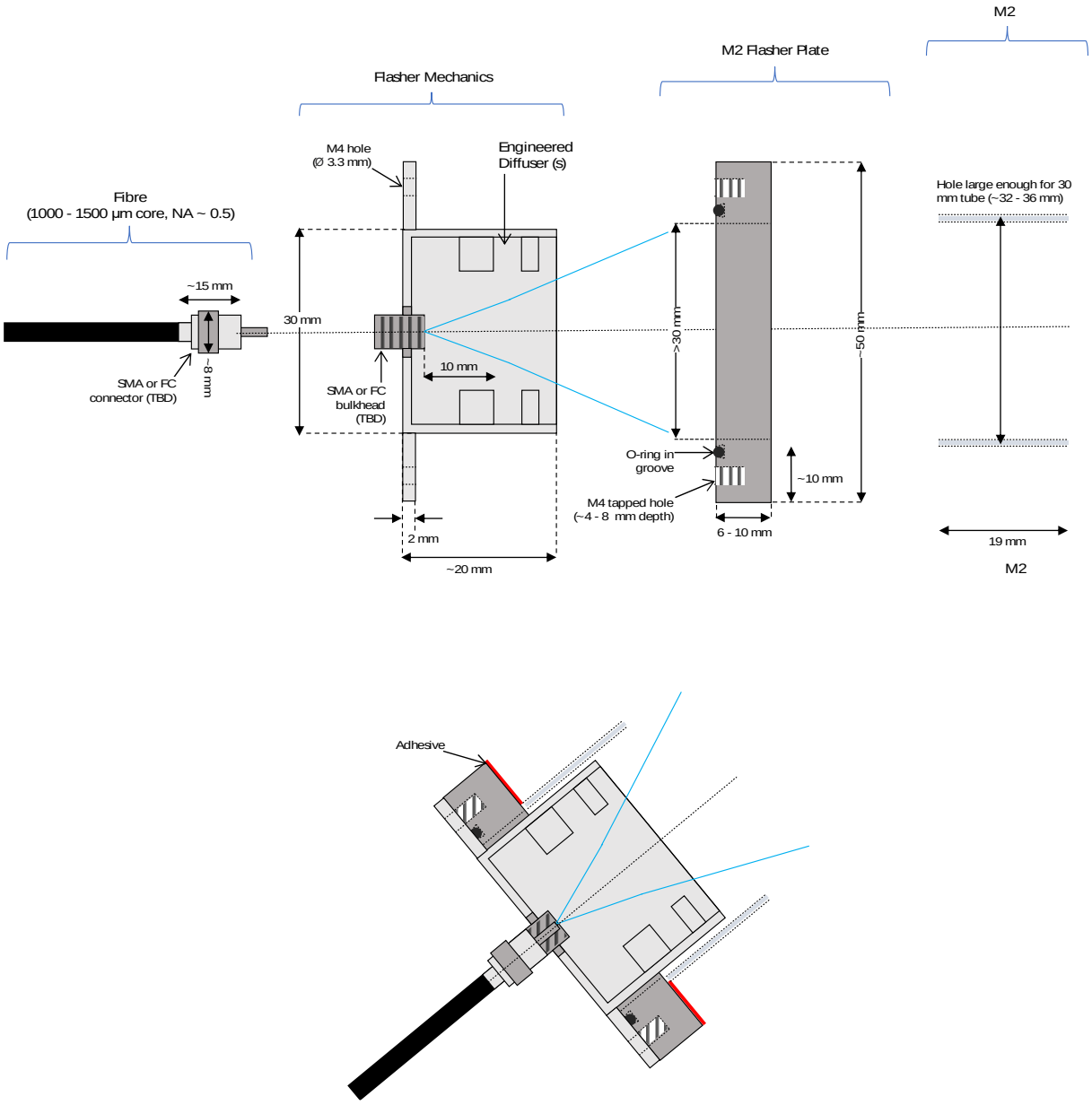


Figure 65: Sketch of flasher mechanics coupled to M2.

The M2 contains a ~30 mm diameter hole at the centre (exact size TBC). A mounting plate is attached to the rear of the M2, with a matching centre hole, at the same time as (and using the same adhesive) as the actuator plates. This mounting plate contains an asymmetric, tapped, bolt pattern to mount the

flasher mechanics and an O-ring in a self-retaining groove. An asymmetric bolt pattern ensures the flasher mechanics are mounted in a known orientation.

The flasher mechanics consist of a machined aluminium piece, with an outer ring containing through-holes to match the bolt pattern on the M2 plate, and a central tube to house diffusers and a fibre bulk-head connector. Diffusers are secured with adhesive, and mechanically locked in position at the time of assembly. An anodised, black, finish prevents excess reflections within the tube.

Two engineering diffusers are combined to provide a uniform beam. The nominal diffuser choice consists of a square, 50° (+/- 25°) diffuser (Thorlabs/RPC ED1-S50) coupled via a small air gap to a 5° (+/-2.5°) diffuser (RPC EDC-5-18397-A). The second diffuser is used to smooth the response of the first, resulting in a more regular pattern. Figure 66 shows the 1-dimensional distribution of light from each diffuser (black: 50°, blue: 5°) as well as the convolution (red).

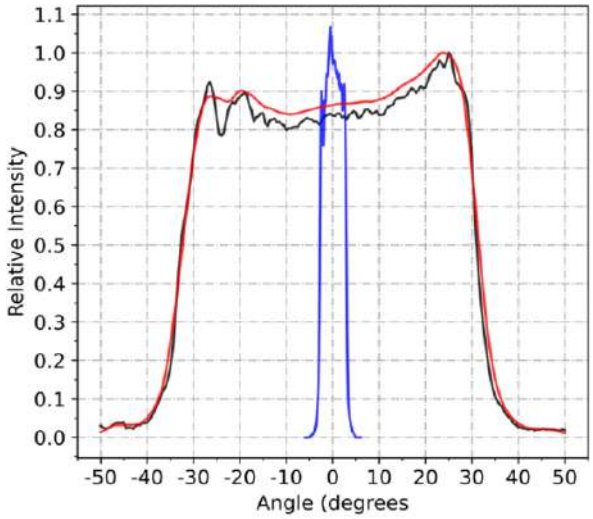


Figure 66: The effect of combining diffusers. Response of 50° diffuser in black, 5° diffuser in blue and the convolution in red. Thorlabs & RPC data, taken via a radial scan.

7.7 Software and Firmware

The software used to control the CHEC camera consisted of four modules, mainly written in C++, called TargetDriver, TargetCalib, TargetIO, and CHECSInterface. The first three modules form the so-called "TARGET Libraries" and are shared with other users of the TARGET ASICs around the world. They were low-level libraries implementing the functionality needed to control, calibrate and write the data that the TARGET Modules produce. The CHECSInterface module contained the programs needed to actually operate the camera: the control service, the logging and monitoring system, the event builder. These programs were linked to the TARGET libraries. The software for the analysis of the data was completely separate still, and doesn't depend on any of these libraries. This control software was successfully used in the lab and the field to test and validate the two CHEC prototypes, CHEC-M and CHEC-S. Several person-year worth of coding went into the development.

To account for the changes in hardware, address the shortcomings identified during internal code reviews and usage in the field, and to meet the requirements in quality and functionality required for CTA, the CHEC-S software will be transformed into a new control software package to be employed in the SST Camera. Specifically, the improvements included will be:

- A formal software architecture design and implementation plan, a modern development model and a more capable build/test/deploy framework will be used.
- The software modules will have more granularity, and be easily extendable. Each module will have a clear scope, associated with the hardware item it controls or high-level operation it manages.
- The software for each hardware item will contain a hardware abstraction layer, to decouple the high-level interface from its low-level implementation. This layer is then wrapped with gRPC to provide Inter-Process Communication capabilities between the individual hardware control processes and the camera manager.
- Along with this, an agreed-upon Information Model for the whole SST Camera will be adopted. This will address the statefulness and incompleteness of the configuration model used in CHEC-S. It will also allow a more fine-grained control of the camera for maintenance/testing purposes.
- We will move away from the TARGET libraries, refactoring the code contained to fit into the new software architecture, while at minimum retaining the knowledge and functionality that was gained in their development.
- An in-depth reference documentation will be provided.
- A full-fledged unit and integration framework will be adopted, that will allow continuous integration tools to be used.
- Emulation of low-level hardware interfaces through the use of "software mocks".
- Integrated firmware testing. Synthesized logic will be verified and will be interfaced to the low-level software using a digital logic verification framework such as cocotb.
- The SST Camera software will be limited in scope, only fulfilling the purpose of controlling the camera and monitoring its status. No code that goes beyond this goal (feature creep) will be written. Suitable off-the-shelf commercial/open source libraries from reputable vendors will be used if needed.
- Safe coding and ops practices are going to be enforced, such as defensive coding and fuzz testing.
- The primary programming language of the software will be Python. Areas which require highly optimised code will be written in C++, and wrapped with the pybind11 library.

The firmware used on the Slow Control Assembly GECCO will be a refactored, expanded version of the one developed for the Slow Control Board of CHEC-S. The TARGET Module firmware will have an AXI/Aurora communication layer instead of the current Ethernet/UDP one; the rest will stay essentially the same. The Backplane firmware will be written anew because of the new L1 and L2 FPGA layout, but it will include code from the previous versions.

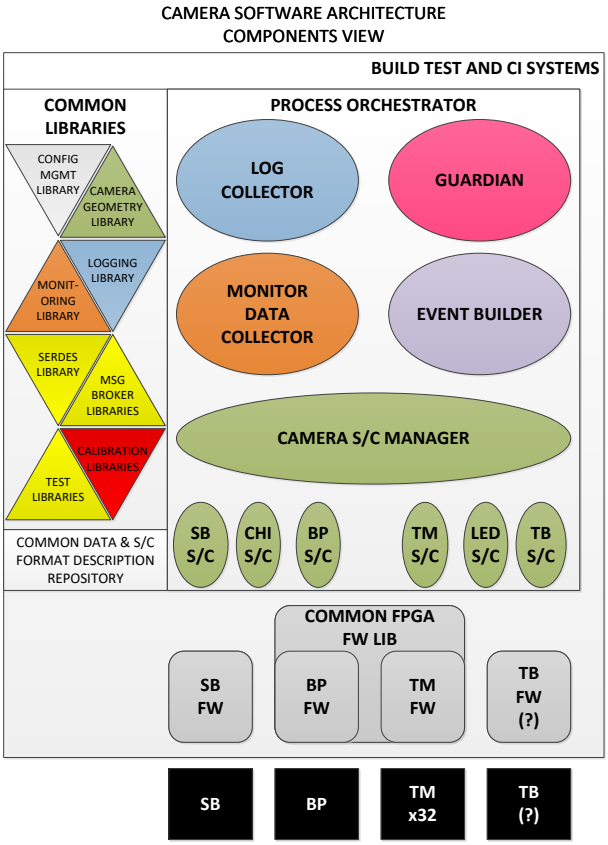


Figure 67: Components of the SST Camera software.

A scheme of the foreseen components of the camera software is given in Figure 67. A build system combining setuptools and scikit-build (setuptools + CMake) will be utilised for convenient installation of the software.

The following libraries will be developed as dependencies to the majority of the camera software, providing common functionalities to the codebase:

- protobuf: defines the message format and gRPC services, providing each process the means to communicate with the other processes.
- telemetry: defines the common telemetry logging API, for the collection of monitoring, configuration events and log messages.
- mapping: defines the geometries of the camera, such as the camera pixel positions, and the conversions between different relevant coordinate frames
- waveform: defines the serialised data format for the waveform data received from the camera, the to-disk io for the raw packets, and the calibration methods.

The following service programs will be built on top of these libraries:

- **eventbuilder**: provides the service to collect, build and perform on-line analysis of events
- **slowsignal**: provides the service to collect, build, re-publish of slow signal data
- **telemetry-collector:** provides a service to collect and re-publish the telemetry
- **orchestrator:** it is a service that starts and stops other camera services
- **guardian:** it is a service that checks the safety of the camera and sends alarms
- **pointing:** service which performs online telescope pointing reconstruction from the slow signal data
- **slow control (S/C):** there will be several interconnected camera slow control services, offering gRPC interfaces and controlling the underlying hardware devices:
    - **camera manager:** provides the service that controls the camera and exposes a simplified, CTA-state-machine-compatible interface (see Section 11.1.1).
    - **slowboard**: provides the server that controls the slow control board
    - **backplane:** provides the service that controls the backplane
    - **chiller:** provides the service that controls the chiller
    - **target:** provides the service for controlling a target module in a single-module setup
    - **flasher:** provides the service that controls the LED flashers

8 Technical Budgets

In this section the Camera mass, power and data-rate budgets are given. In future, the technical budgets may be split to a dedicated document, and additional budgets added (e.g., mechanical tolerances).

8.1 Mass

The Current Best Estimate (CBE) for all Camera Unit elements are given in Table 12, most are from CAD models and therefore accurate. A Maximum Estimate Value is also given, reflecting the current level of uncertainty. The chiller mass depends on the choice of chiller and ranges from ~100 to ~180 kg.

Table 12: Camera Unit mass estimates.

Item	CBE Mass (kg)	# Per Camera	CBE Total Mass (kg)	MEV Total Mass (kg)
Enclosure			**39.6**	**43.5**
Frame Assembly	13.3	1	13.3	14.7
Telescope Plate Assembly	7.1	1	7.1	7.8
Power Panel Assembly			7.9	8.7
Enclosure Panel A	3.5	1	3.5	3.9
PSU (24 V)	2.5	1	2.5	2.8
PSU (SiPM)	1.9	1	1.9	2.1
Heat-Exchanger Panel Assembly			6.3	7.0
Enclosure Panel B	2.5	1	2.5	2.8
Heat-Exchanger Assembly	3.8	1	3.8	4.2
Fan Panel Assembly			4.9	5.4
Enclosure Panel C	2.5	1	2.5	2.8
Fan Assembly	2.4	1	2.4	2.6
FPA			**31.1**	**34.3**
FPM Assembly			11.1	12.2
FPP	7.5	1	7.5	8.3
Thermal Break	0.14	1	0.1	0.2
Transition Plate	2.5	1	2.5	2.8
Rack Interface Plate	1.0	1	1.0	1.0
Door Assembly			13.2	14.6
Mechanics	4.4	2	8.9	9.8
Motor & Gearbox	2.2	2	4.4	4.8
Window Assembly	3.3	1	3.3	3.6
SiPM Assembly	0.04	32	1.2	1.4
FPE Assembly	0.07	32	2.3	2.5
TARGET Module			**8.0**	**8.8**
ERA			**8.7**	**10.6**
Rack Assembly	6.5	1	6.5	7.1
Backplane	1.4	1	1.4	1.5
Slow Control Assembly	0.5	1	0.5	1.0
ERA Cabling and Connectors	0.2	1	0.2	0.5
Timing Board	0.2	1	0.2	0.5
Flasher Assembly			**0.5**	**0.8**
Other			**3.4**	**4.8**
Liquid	3.4	1	3.4	4.8
		Total	**91.3**	**102.7**

8.2 Power

The power consumption of the Camera Unit and the Camera Chiller are given in Table 13. CBE and MEV are provided for several operational scenarios. The MEV under peak conditions reaches a level very close to the power supply capacity, which may be mitigated by reducing doors speed (or operating only one half at a time – total open/close speed still <40 s). It should be noted that chiller values are rough estimates only, and depend on the final chiller choice (here, a worst-case has been assumed).

Table 13: Power consumption estimates. Note: Chiller estimates are very approximate (to be measured soon).

		CBE						MEV					
		Night				Day		Night				Day	
Item		Standby	Observing (typical field)	Observing (max. field)	Peak	Typical	Peak	Standby	Observing (typical field)	Observing (max. field)	Peak	Typical	Peak
Enclosure													
	Fans	104			115	92	115	109			121	97	121
	Fan Controller	10			10	10	10	20			20	20	20
FPA													
	Door Motors				200		200				400		400
	SiPM Assembly		80	276	276				88	304	304		
	FPE Assembly	154	230	307	307			169	253	338	338		
TARGET Module		460	460	460	460			483	483	483	483		
ERA													
	Backplane	48	48	48	48			58	58	58	58		
	Slow Control Assembly	24	24	24	24	24	24	29	29	29	29	29	29
	Timing Board	8	8	8	8			10	10	10	10		
Flasher Assembly		24	24	24	24			29	29	29	29		
Total Camera Unit		**832**	**874**	**1147**	**1472**	**126**	**349**	**907**	**950**	**1250**	**1791**	**145**	**570**
PSU Load	24V-AUX	24	24	24	24	24	24	29	29	29	29	29	29
	24V (1500W)	808	770	847	1172	102	325	878	833	918	1458	117	541
	48V (600W)	0	80	276	276	0	0	0	88	304	304	0	0
Chiller		2000	2000	2000	3000	1200	3000	2400	2400	2400	3600	1440	3600
Total Camera Unit & Chiller		**2832**	**2874**	**3147**	**4472**	**1326**	**3349**	**3307**	**3350**	**3650**	**5391**	**1585**	**4170**

8.3 Data Rate

CBE and MEV data rates are presented in Table 14 for the expected array trigger rate, the required readout rate for a single camera, and a 'burst' rate (incurred for short calibration runs taken at the maximum rate the camera is capable of).

Table 14: Data rate estimates.

Parameter	CBE	MEV	Unit	Note
TARGET Module Data Size				
Number of samples per pixel	128	128	samples	Configurable
Bytes per sample	2	2	bytes	
Pixels per packet	32	32	pixels	Configurable
Packet Header	118	118	bytes	
Packet size	**8310**	**8310**	**bytes**	
Camera Event Size				
Number of pixels in camera	2048	2048	pixels	
Packets per event	64	64	packets	
Total event size	**531840**	**531840**	**bytes**	
Expected Event Rate (assuming array trigger)				
Expected array trigger rate	350	400	Hz	341 Hz in Prod-4 MC
Additional local pedestal triggers	10	20	Hz	Maximum expected (10 Hz nominal)
Additional local flasher-illumination triggers	10	20	Hz	Maximum expected (10 Hz nominal)
Additional local muon candidate triggers	10	20	Hz	Rough upper limit
Total expected event rate to OES	**380**	**460**	**Hz**	
Implied data rate	**1.62**	**1.96**	**Gb/s**	c.f. CTA Requirement of 2Gb/s (B-SST-1450 Camera Output Data Rate)
Maximum Sustained Event Rate (assuming no array trigger)				
Required max. event rate	600	660	Hz	Following CTA requirement (B-SST-1280 Event Rate)
Implied data rate	**2.55**	**2.81**	**Gb/s**	
Maximum Burst Event Rate (<30 s)				
MC expected array trigger rate	1200	1200	Hz	Maximum that the Camera Unit can transport
Implied data rate	**5.11**	**5.11**	**Gb/s**	

9 Technical Development Status

In this section the status of the technical development of each Camera subsystem is briefly described. This section may be removed once the design is complete and proven.

9.1 Enclosure

The ENC CAD is complete and has been internally reviewed by the camera team. Critical features, such as the O-ring design and retention, have been tested (see Figure 68). All COTS items have been ordered, and parts are being manufactured. The first full ENC should be complete in 2022. Final connector positions will be revised, and any lessons learnt from the first ENC incorporated, in early 2023.

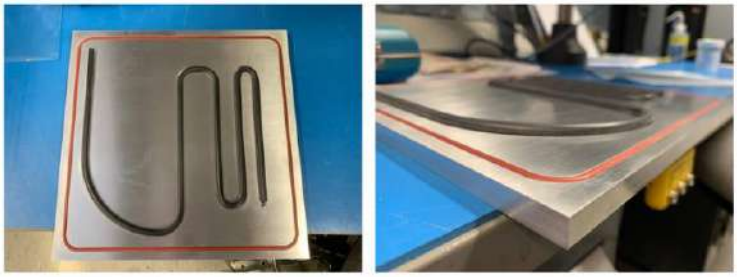


Figure 68: ENC O-ring retention test piece.

9.2 Focal Plane Assembly

FPM. Following the development of FPP test pieces (Figure 69, top), built and extensively tested to verify the weld design, an initial version of the full FPP has been built and leak tested (see Figure 69, bottom). All other elements of the FPM have been submitted for production.

Figure 69: Top: FPP test piece (front: left & back: right)). Bottom: Full FPP (left), and under leak test (right).

Window. Several copies of full-camera window glass have been coated and tested for transmission and uniformity. The window frame has been produced in house, and glass has been mounted successfully (Figure 70, left). A transport container has been designed and produced and has been tested to ship the window from the UK to Germany (Figure 70, right).

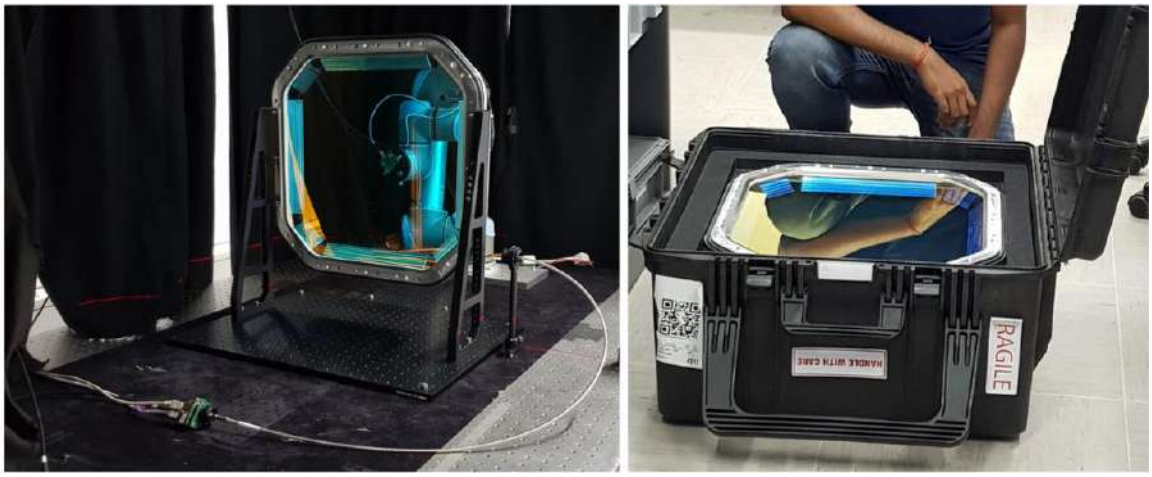


Figure 70: Left: Window Assembly (glass mounted in frame) under test at MPIK. Right: Window Assembly in custom transport / storage container.

Doors. A full set of doors, including hinges have been produced and are attached to motors and dummy FPP for testing and development of the control algorithm (Figure 71).

Figure 71: Left: First set of doors on the bench. Right: Small door half with motor, mounted to dummy FPP & Window Frame.

SiPMs. The choice of SiPM technology has been made, and full tiles have been specified with HPK, including a customised PCB. 50 tiles have been ordered and are due for delivery at the start of 2023. Tests on single pixels are continuing, using e.g., the setup at Leicester shown in Figure 72, left. The SiPM Assembly insertion and retention technique has been tested using dummy parts (Figure 72, right). A dedicated adhesive dispensing robot has been procured from Fisnar to reliably attached heat-sinks, custom tools for handling and jigs for attaching heatsinks have been developed (Figure 73).

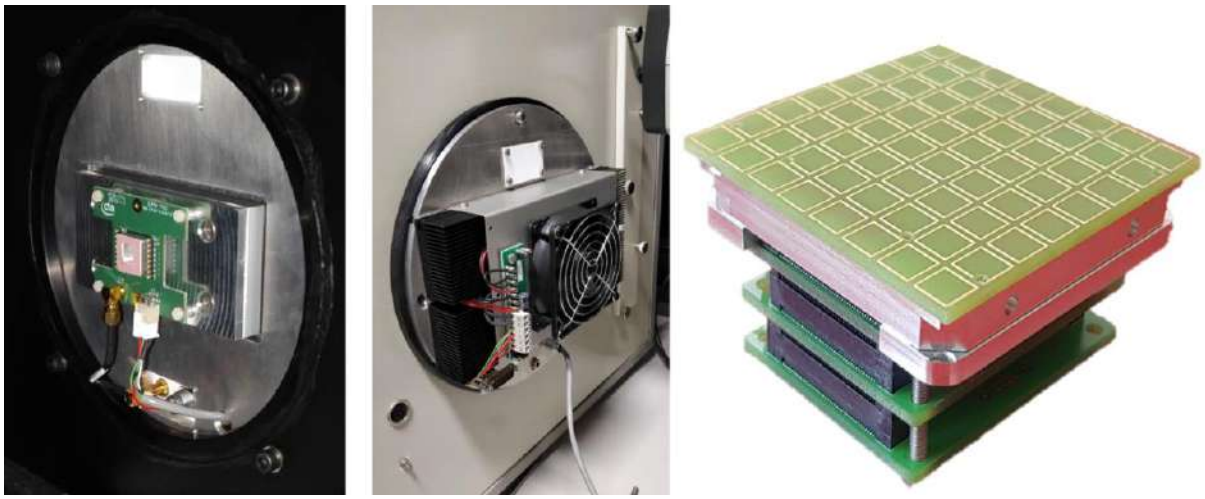


Figure 72: Left & Middle: SiPM test setup with thermal control at the University of Leicester, with single SiPM pixel mounted. Right: SiPM & FPE dummy assembly.

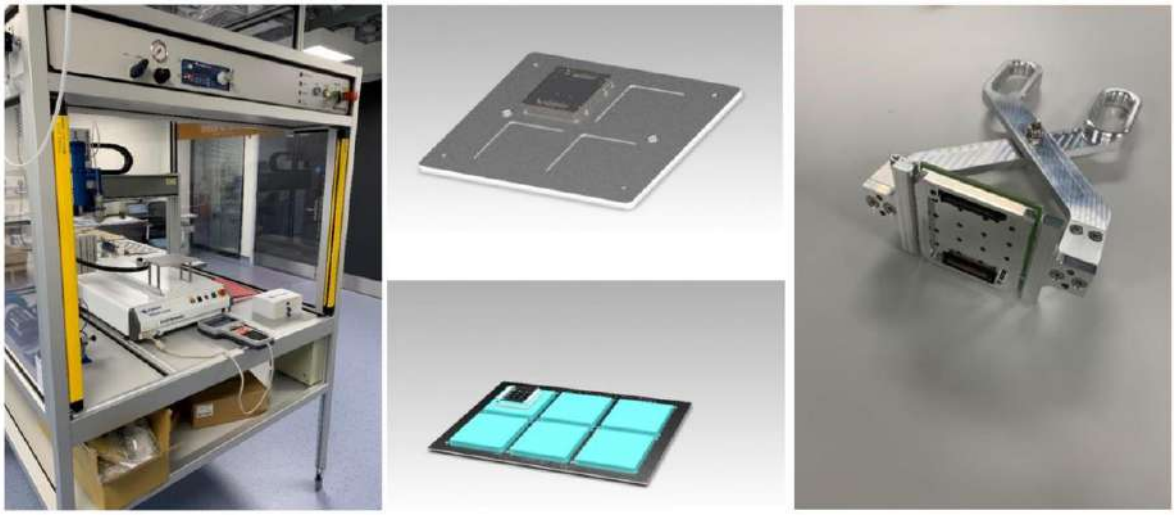


Figure 73: Left: Fisnar adhesive robot, used to dispense epoxy and/or thermal compounds as needed to the SiPMs and FPE. Middle: Custom jigs for holding the SiPMs safely whilst the heatsinks are bonded. Right: SiPM handling tool, for use once the heatsinks are attached (enabling zero contact with SiPM surface).

FPE. FPE R&D is complete and the performance of the FPE coupled to the SiPMs meets requirements. Figure 74 shows the University of Leicester test setup (left), and several measurements (right). The pulse shape behaves linearly with ~10 ns FWHM until an illumination level of ~500 p.e., and then starts to saturate in a predictable way. Figure 75 shows example pulse-height distributions taken with a single SiPM pixel, preamplifier and shaper chain, as measured on a DSO, for input illumination levels ranging from ~1 to 10 p.e. It should be noted that the TARGET ASICs will add some additional noise to such measurements. All FPE PCBs have been designed, reviewed and are about to be ordered. FPE cables have been specified with Samtec and ordered.

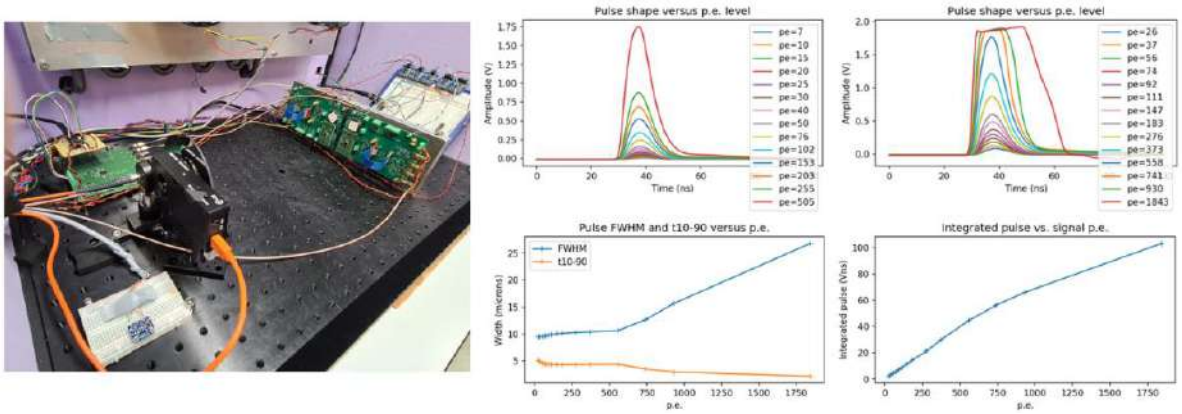


Figure 74: Left: SiPM, preamplifier and shaper tests at the University of Leicester. Right: Resulting performance, showing average pulse shapes from 2 p.e. to ~1800 p.e. Beyond ~500 p.e., once saturation starts to occur, charge-reconstruction will make use of the increasing pulse width.

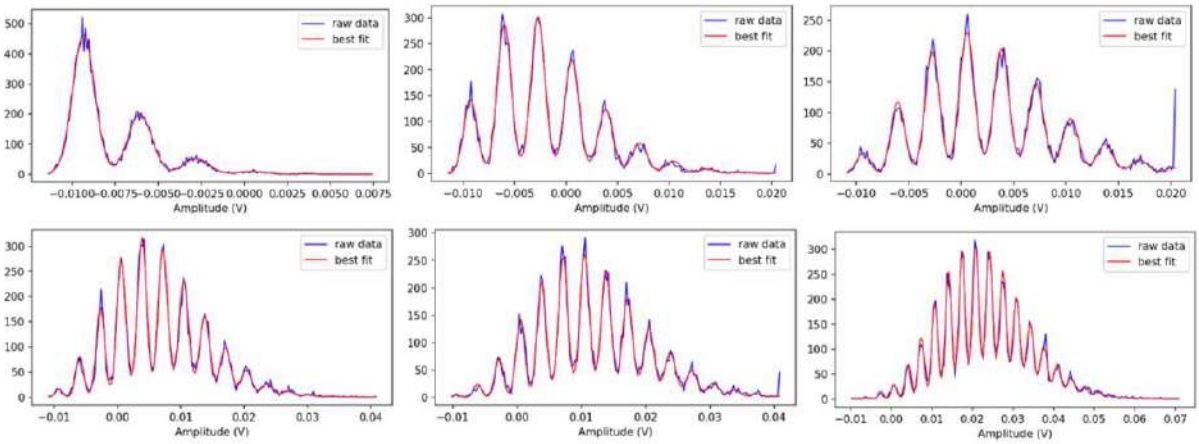


Figure 75: Pulse height spectra for illumination levels of ~1 to 10 p.e. to a single SiPM pixel connected to the preamplifer and shaper chain, as measured by a DSO.

9.3 TARGET Modules

The TARGET Modules schematics and layout are complete and under internal review prior to first production (see Figure 76 for an example layout). Changes c.f. CHEC-S include:

- Usage of the improved TARGET ASICs. TARGET chips from the CHEC-S batch are not available anymore, a new production was kicked off with some minor changes, at a different foundry.
- Removal of EM Faraday cages around components (no benefit was found in CHEC-S). This leads to better airflow and a lower temperature gradient across the ASICs.
- Revision of connectors to the FPE.
- Bias voltage generation circuitry moves out of the TARGET Module to the Bias Board on the FPE, with individual pixel HV control.
- Addition of a low jitter local oscillator for FPGA transceiver clock (relaxes requirements for Backplane clock distribution network).
- Additional on-ASIC temperature sensors. Leads to better TARGET ASIC calibration
- Use of AXI/Aurora communication instead of Ethernet UDP packets.
- The sync and trigger signals are made high-speed source-synchronous by repurposing an unused LVDS line to the backplane as their synchronous clock.

- The enable signal from DC/DC converter is routed to the backplane connector instead of being shorted to +12V. Improves power sequencing of TARGET Module.
- Route the OneWire Unique ID chip signal to backplane connector pin.
- Change the offset of the DC-coupled Slow Signal Measurement.

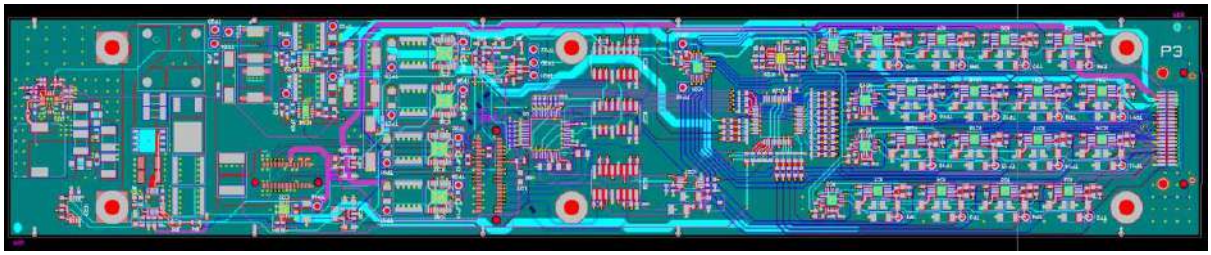


Figure 76: Latest TARGET Module Power Board layout.

The risks associated with these changes are fairly minor, chiefly increased electronics noise, resulting in a reduced signal-to-noise ratio and ultimately worse camera performance. The main mitigation has been early prototyping. All aspects of the TARGET Module performance have now been verified with CHEC-S and/or on evaluation boards. The latest ASICs, optimisation of ASIC parameters, firmware and calibration procedures are actually providing improvements in performance (see Figure 77). Following production of the first modules (expected early 2023), test will take place as part of full Camera Modules; each consisting of: an SiPM Assembly, a FPE Assembly and a TARGET Module (see Figure 78).

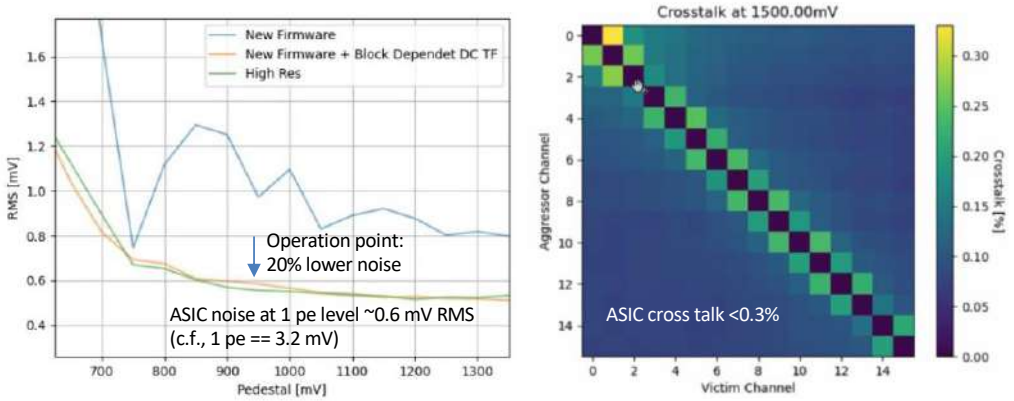


Figure 77: Examples of recent ASIC performance measurements. Left: RMS noise level vs. chosen operating pedestal. Right: Electrical crosstalk.

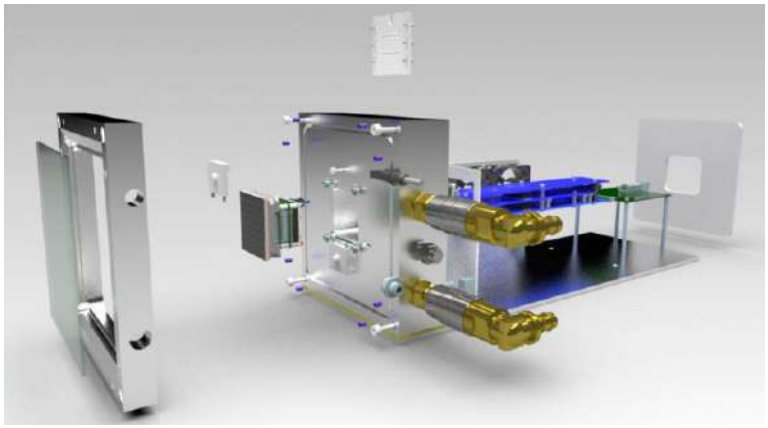


Figure 78: Single Camera Module test rig.

9.4 Electronics Rack Assembly

Rack. An initial version of the rack design is complete, and under manufacture. The initial version does not include cable routing points, these will be added by hand during the QCAM build process. The rack design will then be updated with the mounting points, and any other changes needed.

Backplane. A ¼ Backplane (QBP) has been produced (Figure 79) and is under test at DESY. Essential electrical checks have been completed and firmware development has begun. Once functionality is confirmed, the design will be expanded to the full Backplane. The QBP is suitable for use in QCAM, the full BP is needed for ECAM.

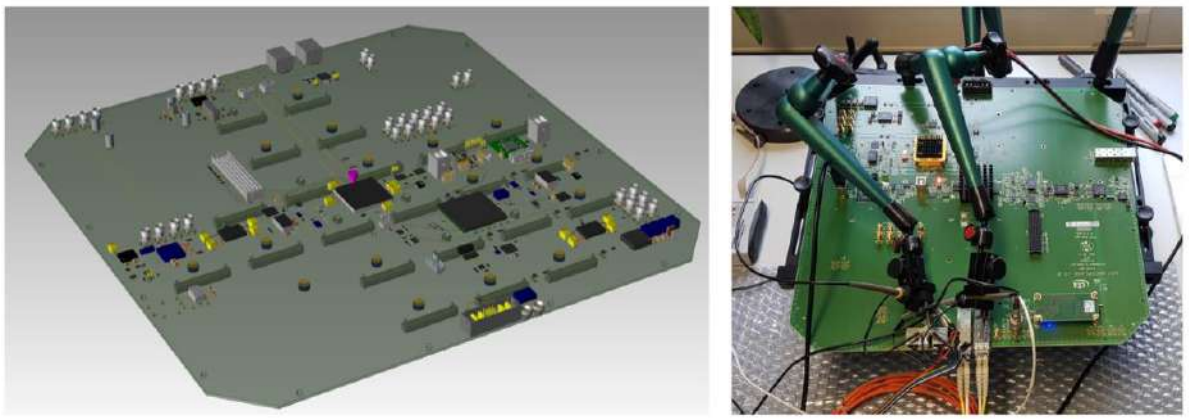


Figure 79: QBP CAD (left), and under-test on the bench (right).

Timing Board. No changes to the Timing Board are needed. Several copies exist and are ready for use.

Slow Control Assembly. The Slow Control Board initial design is complete, and PCBs have been procured (Figure 80). Population of the PCB will take place in a staggered fashion, checking the functionality of each section of the board at a time. GECCO boards exist and have been tested. Motor controller boards (and spares) for QCAM & ECAM have been procured and tested using an evaluation board (as part of the door test setup).

Figure 80: Slow Control Board, ready for population.

Cabling. All long-lead cables for QCAM have been ordered, others will be made in-house. Initial cabling will be done on QCAM, and then cable lengths and mounting points will be decided. Following this, custom length cables will be ordered for ECAM, and retrofitted in QCAM if desirable.

9.5 Flasher Assembly

The v3 flasher performance has been measured, including long-term stability. The v4 changes are underway, with the first daughter boards produced and ready for testing. GECCO boards exist and are ready for use with the mother board, which is under design for production in early 2023.

9.6 Camera Support Systems

Chillers have been ordered and are ready for delivery for testing in Adelaide and Leicester. Power and fibre cables have been procured, ready for testing with QCAM, Lab tests are underway to verify fibre coupling to the M2.

10 Camera AIT

This section gives a brief overview of SST Camera AIT steps prior to arrival on-site at CTAO-South. Focus here is on design-features, not detailed procedures. Further AIT details will be provided in the Camera Series-Production Plan [RD9], and AIT of every subsystem will follow a detailed procedure.

The SST Camera is designed to allow the major camera subsystems (ENC, FPA, TM, ERA) to be assembled independently, before integration. This achieves an efficient parallelisation of work. This scheme also ensures that the uncoated SiPMs are mounted inside the sealed FPA at an early stage, thereby protecting them. The assembly concept reflects the line-replaceable unit philosophy of the camera PBS and is optimized not only for production but also for maintenance. Upon assembly, the full camera will undergo pre-shipment verification tests before shipment to CTA-South and integration into the SST structure, as described in [RD11].

Figure 81 shows an overview of the camera integration steps, described in more detail below.

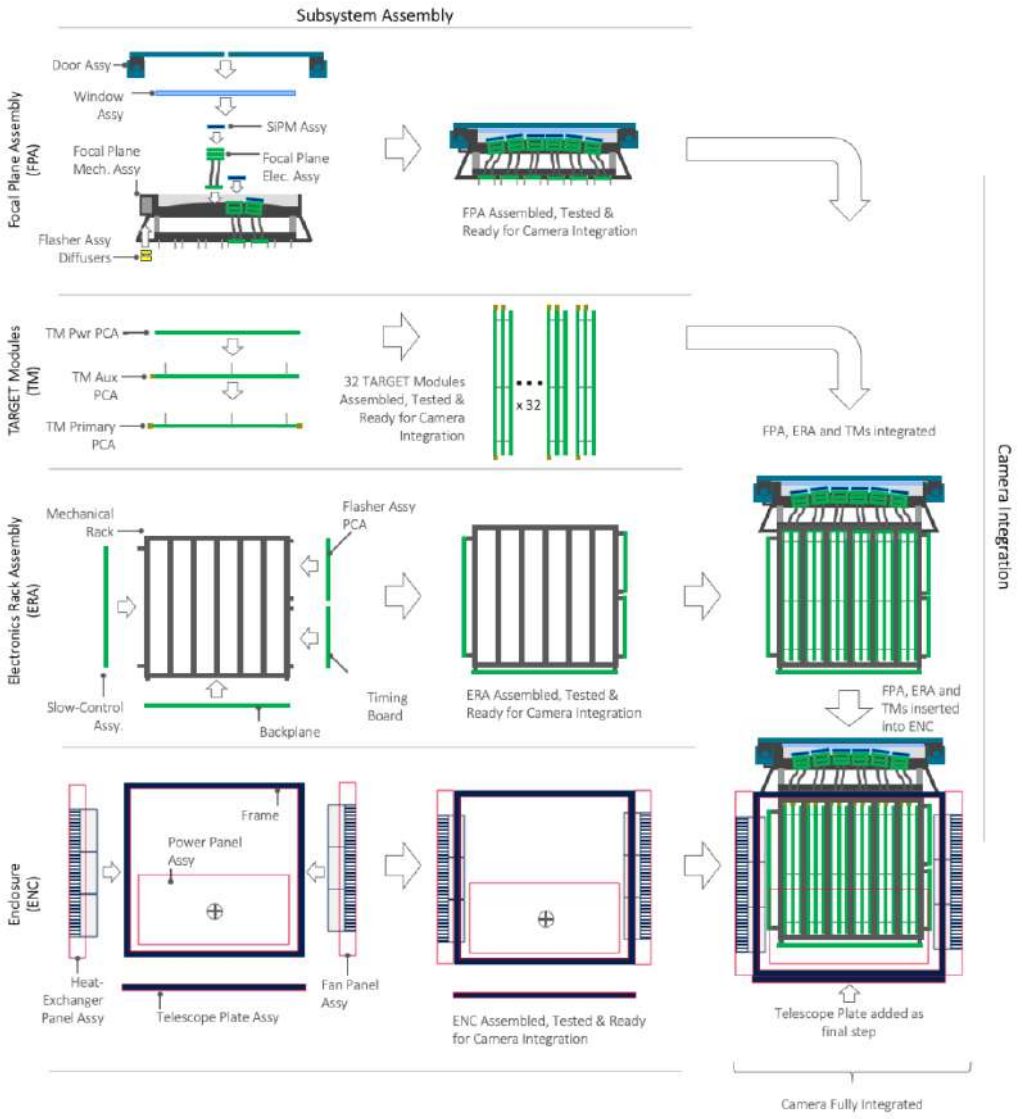


Figure 81: Schematic illustration of the assembly procedure. Individual elements (left) are assembled into subsystems (centre), which are then integrated, in the order shown, into the complete camera (lower right).

10.1 Subsystem AIT

10.1.1 ENC

The ENC frame will be welded together by a commercial partner following in-house part production at MPIK. All parts include orientation markers. The frame and all panels will also be finished (anodised and painted) commercially. O-rings will be fitted to the frame at the time of ENC assembly. The fan, heat-exchanger and power panels will be assembled in batches and functionally tested prior to ENC integration. ENCs will be assembled prior to camera integration. Leak tests will be performed using a blanking plate in place of the FPA. The desiccator will be fitted, but the desiccant only added at the time of camera integration. ENCs will be stored fully assembled at MPIK awaiting camera integration.

10.1.2 FPA

The FPA is the most complex camera subsystem and requires a suitable site for integration, nominally chosen to be Groningen. Prior to integration the following elements are produced.

- Focal Plane Mechanics: Produced in-house at MPIK, with the FPP welded by a commercial partner. The FPP will have liquid connectors and all other hardware fitted, and then will undergo leak tests prior to delivery to the FPA integration site.
- Window: The window glass is procured to size and coated by a commercial partner in the UK. The company provides measurement of transmission vs angle and wavelength for all units before delivery to a camera institute. The window frame is machined in house. Sponge seals are used between the frame and the glass to mitigate thermal expansion (Figure 82). The Finsar adhesive robot is used to bond the sponge seals to the glass and frame. A custom container is used to ship the Window Assembly to the FPA integration site.

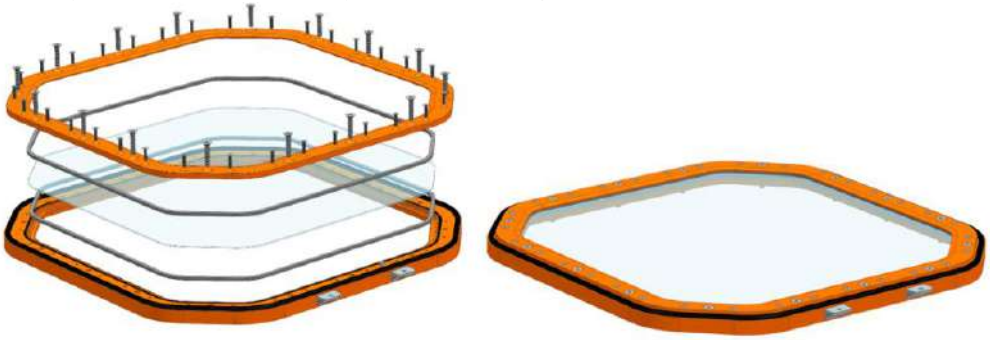


Figure 82: Window Assembly, showing glass sandwiched between two flexible seals.

- Doors: Mechanical pieces will be produced in house, and combined with the COTS motors on a test rig prior to delivery to the FPA integration site.
- SiPMs: SiPMs will undergo testing prior to shipping. Heatsinks will be attached and the SiPMs will be handled and transported to the FPA integration site following the procedures described in Section 7.2.4.5.
- Focal Plane Electronics: The FPE PCAs will be produced by a commercial partner and electrically tested prior to delivery to camera partners, where they will undergo heat-sink attachment, assembly from boards to sets of FPE, and further tested. Sets of FPE Assemblies will then be delivered to the FPA integration site.

Once all elements are available, integration into the FPA can take place. The Focal Plane Mechanics include a pair of dedicated lifting points that will be used to secure them to a jig, allowing the following steps to then be followed:

- Attach FPE:
    - A FPE Assembly without cables and TM Interface board is inserted into the front of the FPP, through the cut-outs.
    - The FPE Assembly is then locked in place using the clamps (see Figure 83).
    - This is repeated for all 32 FPE Assemblies

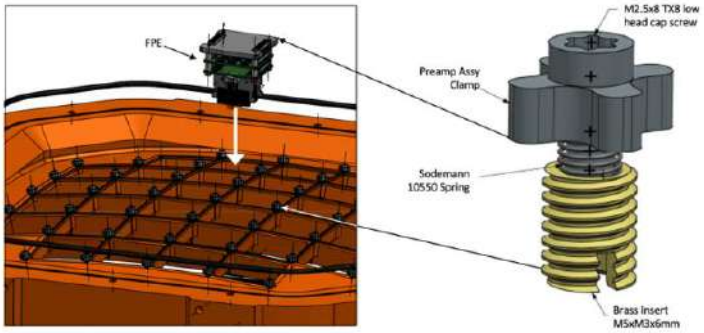


Figure 83: FPE retention mechanism.

- Mount the SiPMs:
    - Within each FPE Assembly, the Bias, Preamp and Cable Interface boards are held together via 4 screws that connect the boards via hollow spacers. Two of these screw holes reach all the way though the preamplifier heat sink and must be removed to attach the SiPMs. See the red screw heads in Figure 84Figure 32.

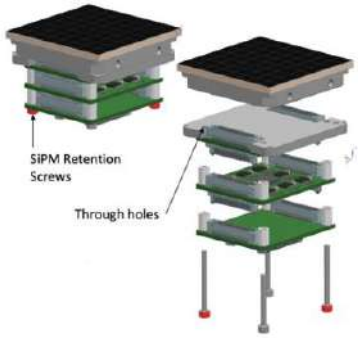


Figure 84: SiPM retention mechanism.

    - One person inserts two “SiPM mounting screws” into the now empty screw slots in the FPE Assembly from the back. These screws protrude through the focal plane, and offer up a mounting point “above” the neighbouring FPE for SiPM attachment.
    - Using the SiPM handling tool, a second person offers up the SiPM Assembly to the protruding screws. Person one then rotates the screws into threaded holes on the rear of the SiPM Heatsink.
    - Person one, then gently moves the screws backwards, pulling the SiPM Assembly into position until it mates with the connectors on the FPE Assembly.
    - The SiPM mounting screws are removed, and replaced with screws of the correct length. The SiPM Assembly is thereby locked into the focal plane.
    - This is repeated for all 32 SiPM Assemblies
    - The Kapton tape is removed from the front of the SiPM Assemblies once they are all in the FPP (TBC based on risk tests).
- Mount the Window Assembly:
    - The Window Assembly is attached to protect the SiPMs. A thin protective pad may be added to avoid marking or damaging the glass in the remainder of the activities.
- Attach FPE Cables and TM Interface Boards:

- All 32 sets of FPE Cables and TM Interface Boards are then attached and secured via spring mount to the Rack Interface Plate (see Figure 85).

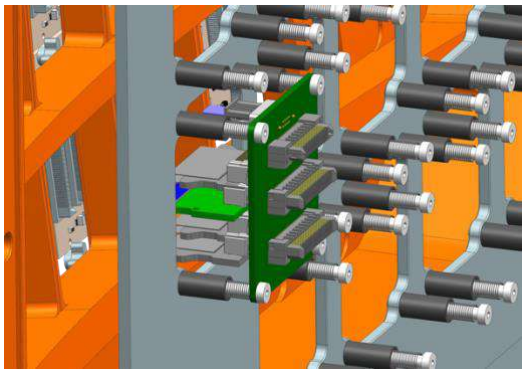


Figure 85: Rack interface plate with spring-loaded stand-offs and single TM Interface Board attached.

- Door attachment:
  - The doors are attached and roughly by hand.
  - The motors and sensor cables are connected to an alignment system (a set of motor controllers with dedicated firmware and corresponding software) and precision alignment is done.
  - Cables are detached from the alignment setup and routed through the Transition Plate via water-tight gromets (Figure 86).

Figure 86: Motor cable routing through Transition Plate via grommets.

- Tests:
  - Using a hand-probe tool, the serial number of each SiPM and FPE Assembly is probed at test points on the rear of the TM Interface Board and the configuration automatically stored in a data base.
  - A single TM or similar probe board, and bench top power supply, is attached to each slot in turn and used to check basic.
- Window screw securing and visual checks:
  - Window frame screws are removed, Loctite added, and then replaced and secured to a specified torque.
  - The FPA is visually inspected before being packed in a dedicated humidity-controlled storage and transport case for delivery to the camera integration site.

10.1.3 TARGET Modules

The TARGET Modules will be produced by a commercial partner and electrically tested prior to delivery to camera partners. The PCB population company will procure all parts, apart from the ASICs, which will be provided by the camera partners. Upon delivery, the TARGET Module PCAs are individually inspected, FW is loaded to the FPGA, and each board undergoes a first stage of testing and calibration.

Modules are assembled from PCAs that pass this first stage. Further tests and calibration data at then taken. All data is matched to the TARGET Module using serial-id chips onboard each PCA. TARGET Modules are sent in batches to the MPIK for integration into cameras.

10.1.4 ERA

The ERA rack parts will be machined in-house at DESY and sent to MPIK as a flat-pack assembly. The Backplanes and Timing Boards will be procured and tested by DESY prior to delivery for camera integration. The Backplane will include easy handling points to avoid damage when attaching to the rack. ERA cables will be made to length, and the rack will include points to secure the cables.

10.1.5 Flasher

The Flasher PCBs will be procured from commercial partners, and electrically tested prior to delivery at Durham University. The LEDs will be soldered in-house to the otherwise complete boards. Prior to attachments, LEDs will be burnt in to ensure stable operation. Each LED Flasher Daughter Board will be tested and calibrated in a thermal chamber to ensure a stable temperature. Calibration data will be stored and associated to the corresponding Flasher Daughter Board later via the on-board unique serial number. Complete Flasher Assemblies will be delivered to MPIK for integration into cameras.

10.1.6 Camera Support Systems

The Chiller, pipework, fibre cable and power cable will all be procured from commercial partners and sent directly to CTAO-South. Copies will be required for camera integration, and for long-term / stress testing at camera institutes.

10.2 Camera Integration

Once the camera subsystems have been assembled and tested as described above, they are delivered to the camera integration site at MPIK. Integration of the subsystems into a full camera requires a dedicated assembly rig, and a temperature and humidity-controlled room. The concept is illustrated in Figure 87 and proceeds as follows.

1. The dedicated assembly jig is visually checked, and the room cleared of.
2. The ENC Frame is mounted to the rear of the assembly jig.
3. All ENC panels are mounted to the assembly jig, suspend / held offset from the frame.
4. The FPA is attached at the front of the jig to a rotating mount.
5. The FPA is rotated such that the doors face down, and the ERA is attached to the rear of the FPP. All motor and sensor cables are connected.
6. The FPA is rotated to allow access to the back of the rack and the TARGET Modules are inserted. The Backplane is secured, and the TARGET Modules are mated to both the FPE and BP as shown in Figure 88. All cables between the Backplane and ERA are connected.
7. The FPA+ERA+TMs are rotated and manoeuvred on sliding rails toward the ENC.
8. The FPA is mated with the ENC and secured. ENC panels are moved into position and cables connected.
9. The FPA mount is retracted. The camera is powered up and quick functional checks made.
10. The camera is powered down and all panels are mated with Loctite on all screws.
11. The camera is purged of moisture and desiccant added to the desiccator.
12. The chiller is connected, and functional checks of the camera are done.

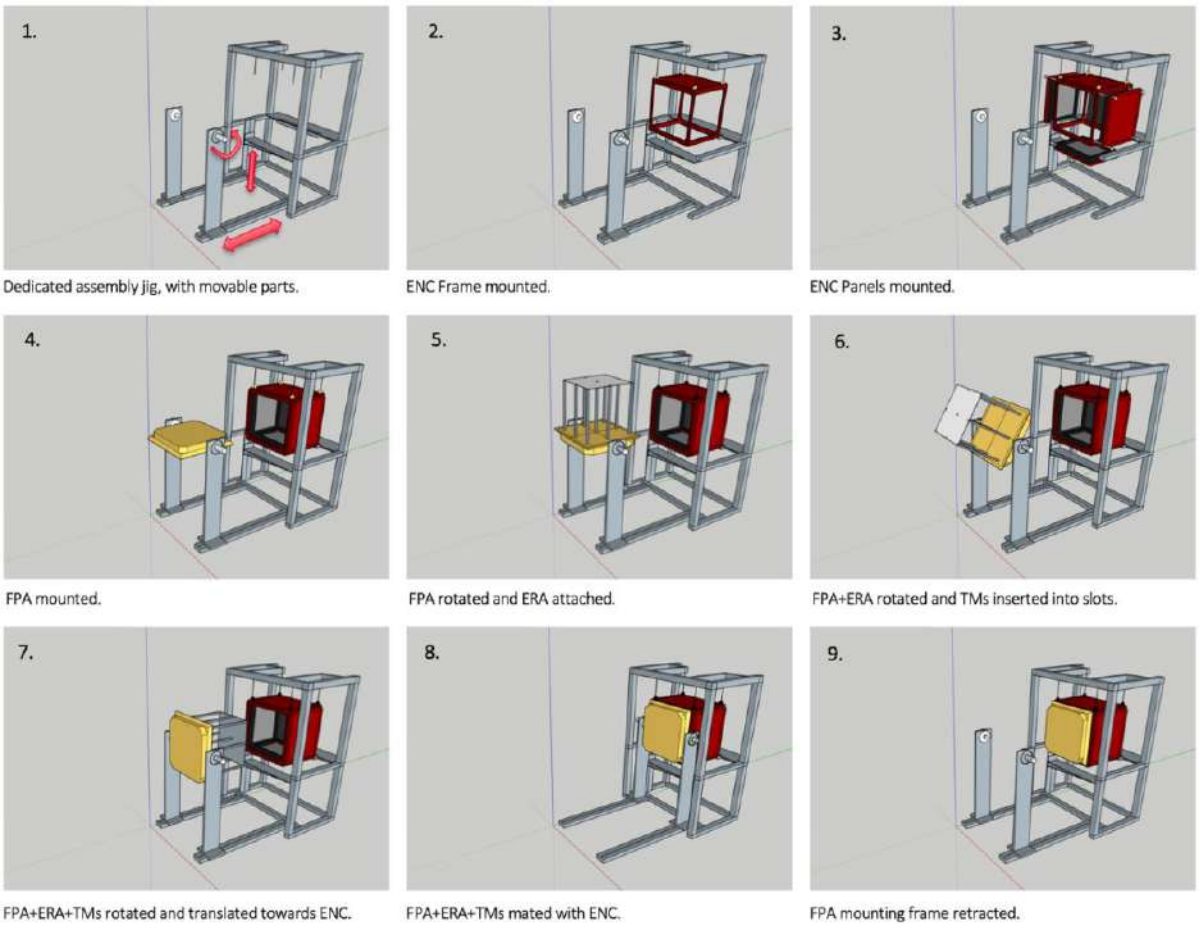


Figure 87: Cartoon showing the camera integration steps. Note: as pictured ENC panels are secured prior to inserting the FPA+ERA assembly, in the text the counter option of securing the panels last is described (both at feasible and will be tested).

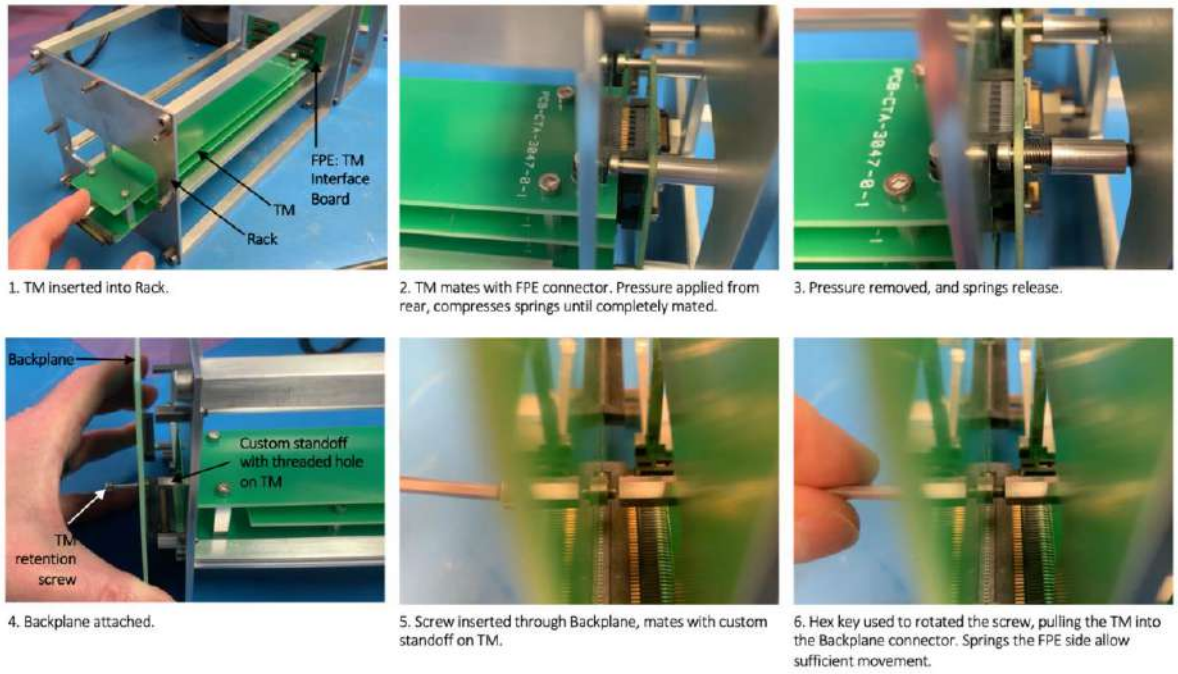


Figure 88: TARGET Module (TM) insertion and retention concept, illustrated using a single slot mock-up of the system.

10.3 Pre-Shipment Verification

Camera elements / subsystems will be inspected, calibrated and tested (as applicable) at contributing institutes prior to camera assembly. Each camera will then undergo a final verification step prior to shipment to CTAO (see [RD9][RD9] for further details). Cameras will be verified against requirements following a detailed test plan and procedures (approved by CTAO at a Test Readiness Review prior to testing). The complete set of tests are to be defined, but will consist approximately of:

Pulse shape: MC simulations show that a pulse shape with 5.5 – 10.5 ns FWHM and rise time 3.5-6 ns is optimal for triggering. The typical SiPM pulse shape is wider than that, so shaping electronics are required to narrow the pulse width. Pulse shapes will be characterized full camera AIT.

Photosensor performance: SiPM performance parameters to be characterised are the photon-detection efficiency (PDE) vs. wavelength, the optical cross talk (OCT) and the dark count rate (DCR). These will be measured during SiPM AIT.

Single photo-electron spectrum: The single p.e. spectrum measurement consists in measuring the distribution of charges recorded by the SiPMs when illuminated with light pulses with an average intensity of ~1 p.e. By fitting the resulting charge spectrum, the gain, relative illumination level, and optical cross talk of each pixel can be monitored. This measurement will be performed during the full camera AIT.

Intensity resolution: The intensity resolution measures how precise is the pixel intensity estimation with varying intensity of illumination. It can be measured by illuminating the camera with a pre-calibrated variable-intensity light source and determining the distribution of the measured light pulse charges. This measurement will be performed during the full camera AIT.

TM & ASIC performance: The noise, time resolution and internal cross-talk of TARGET trigger and sampling ASICs and full TMs are going to be measured as part of the TM AIT.

Saturation: The saturation of the readout chain is measured in the final points of the intensity resolution measurement. As such, it will be characterised as a part of it.

Trigger performance: The minimum coincidence window of the trigger will be measured as part of the Backplane AIV. The trigger signal skew will be measured as part of the Camera AIT.

Data rates and dead time: Readout dead-time and maximum data rate will be measured as part of the Camera AIT.

Window: The entrance window transmission vs. wavelength, angular response and uniformity will be measured during the window AIT procedures.

11 Camera Concept of Operations

This section gives a brief overview of the concept of operation for the SST Camera. The full SST Concept of Operations can be found in [AD6].

11.1.1 Camera State Machine

The SST Camera will honour the ACADA – Generic Telescope Control Interface defined in [RD12], and implement the control state machine defined in [RD13] (Figure 89). In the following, the generic state and sub-state definitions are copied verbatim from that table, with SST Camera-specific additions in *italics*.

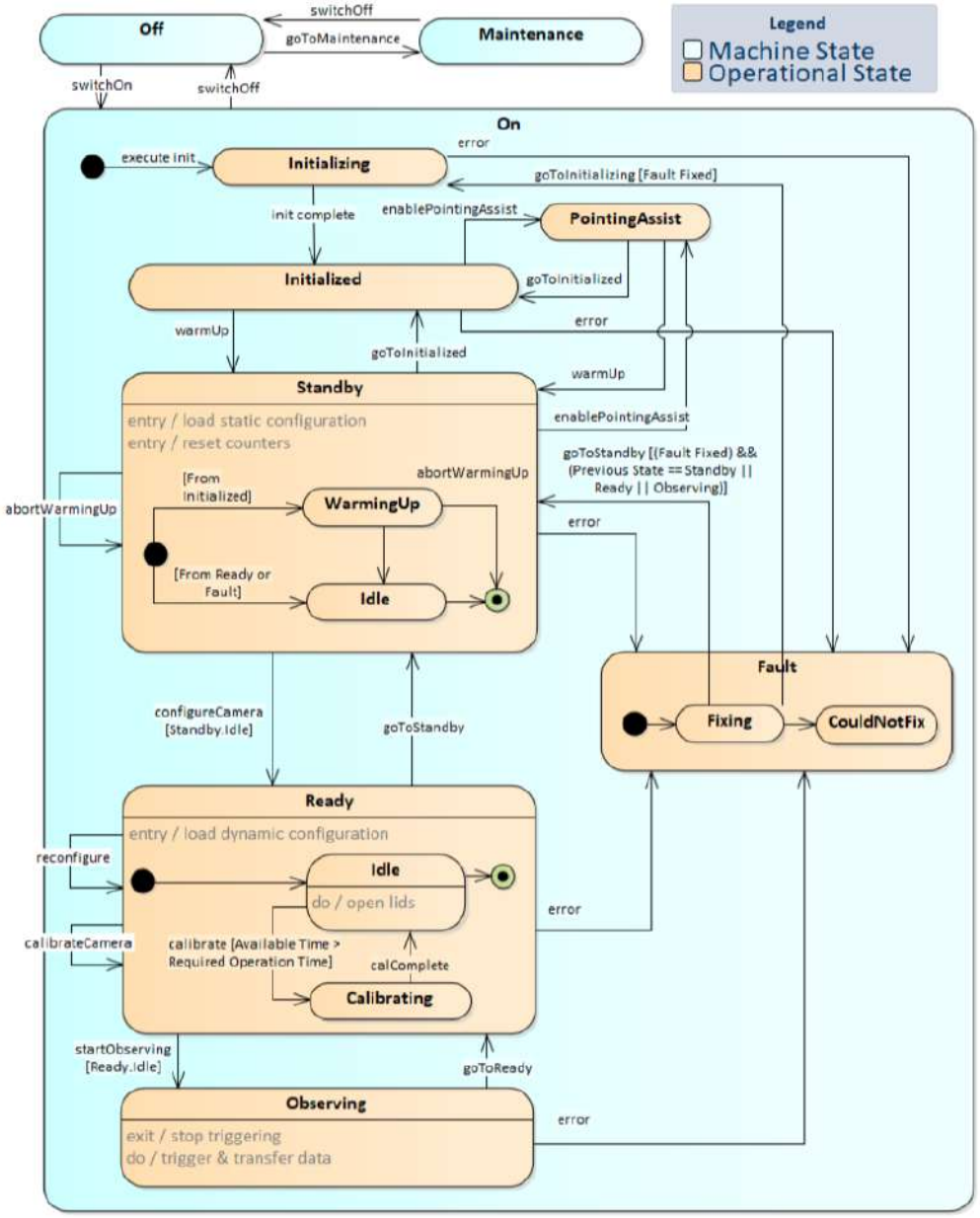


Figure 89: State machine of SST Camera including the states and their sub-states, from [RD13].

Off: This is the state that the Telescope Manager can infer when there is no connection to the Local Control System. If an attempt to power up the Camera results in one of its sub-systems not able to be powered up, the Camera will go to the Fault state, via the **Initializing** state. The SST Camera is completely unpowered, the main 220V AC is off.

Maintenance: The Camera is in a state designed to perform maintenance activities and is unavailable for scientific operations or any kind of remote control. The SST Camera is undergoing maintenance/repair/substitution. This may involve the need to power camera and chiller, move the doors, check fan speeds etc., whilst physically at the telescope. Maintenance of this type is to be accomplished by connecting a laptop running specialized maintenance software to the network cabinet. The maintenance software would then be able to take control the camera. Such command override is only possible in this state. The Camera Manger cannot exit the Maintenance state while the maintenance software has control of the camera.

On: The Camera is switched on, and available to operate under the operational states described below. The 220V main reaches the Power Supplies, and the Slow Control Assembly is powered on by the AUX Power from the 24V Power Supply Unit, which is always connected. Chiller is likewise powered on. Ethernet communication with the camera control software is established.

Operational states within the On state

Initializing: Camera just transitioned to the ON machine state and is initializing all its necessary internal components in order to arrive at the initialized stated. The 24V PSU main power is off. The Slow Control Assembly starts all sensor monitoring loops and starts sending monitoring data to the Camera Server.

Initialized: Camera is in a configuration suitable for survival in extreme environmental conditions, minimising the use of power whilst still providing basic status monitoring and maximising the instrument lifetime. The Slow Control monitors the temperature, humidity, door position sensors. Fans are off. Chiller is idle. If the Slow Control detects that the doors are not closed anymore or the temperature/humidity are in an unsafe state, an error is given and the camera transitions to the **Fault – Fixing** state.

Standby – WarmingUp: The Camera starts immediately the warming-up procedure. The operation can be externally aborted; then the Camera goes back to the **Initialized** state. Otherwise, Camera will self-transition to the **Standby – Idle** sub-state. It the camera is already warmed up when entering in the state, and then it goes immediately to the **Standby – Idle** sub-state. An abortWarming command will then trigger a goToInitialized transition. The Slow Control Subassembly enables the main 24V PSU, establishes I^2C communication with the RSUs and sets the fans at max speed. It then powers on the Backplane, monitoring its in-rush current; then it establishes I^2C communication with it. It then starts the power monitoring routines involving the Backplane. Ethernet communication between the camera control software and the Backplane is set up. The Slow Control then powers on the TARGET Modules one by one. The power-on in-rush currents of the TMs are measured at high frequency for the first second after power-up. Aurora Chip2Chip links between Backplane and TMs are established. The Backplane/TARGET Module/Timing Board synchronization procedure is carried out. The TARGET Module perform their initialization. The TMs power on the Focal Plane Subassemblies. The 48V PSU is enabled, but the Bias Voltage is not applied to the SiPMs. Meanwhile, the Chiller PID controller is set to the nominal operational temperature.

Standby – Idle: Camera is warmed up and ready to go to the **Ready** state. The SST Camera reaches this state when its internal temperature has reached an equilibrium.

Ready – Idle: Camera is warmed up, lids are open, and ready to go to the Observing state. Dynamic configuration is loaded on entry. A self-transition can be triggered to reconfigure the dynamic configuration, which brings the Camera back to the **Ready – Idle** state or triggers an internal calibration depending on the new configuration and time budget. The SiPM bias voltage regulators are enabled, but the bias voltages are set to zero.

Ready – Calibrating: Camera self-calibrating. It can be triggered internally, according to the time budget provided by ACADA for being ready for observations, but can also be externally triggered to start internal calibrations. The calibration runs described in Section 11.1.2**Error! Reference source not found.** can be carried out.

Observing: Camera is acquiring data. Depending on the configuration parameters loaded during the ready state, the camera can be acquiring Cherenkov shower data, dedicated calibration data or shower and interleaved calibration data. The bias voltages are set to their nominal values, the event builder is started, the data acquisition routines are started, the slow signal acquisition starts taking data, the event counters are reset, the event timestamping is enabled, the trigger is enabled, the camera starts taking data.

Fault – Fixing: Camera is trying self-fix the error. After fixing the error, if the Camera was in the **Standby**, **Ready** or **Observing** state, it will try to reach the **Standby** state. In case the **Standby** state cannot be reached, of for the other states before the fault, it goes to the **Initializing** state (which will trigger the transition to go to the **Initialized** state afterwards). If the cancelTransition command is issued, the autonomous fixing procedure is interrupted, and the Camera will go to the **CouldNotFix** state. Example of fault fixing: if the previous state was **Initialized**, and the temperature or humidity inside the camera are outside safe limits, the fans and/or the optional heater are turned on. If the position sensors indicate that the doors are not closed when they should be, the motors controllers are commanded to close the doors. Powering on fans, heater and doors requires the main 24V PSU to be enabled, an action performed autonomously by the Slow Control. The chiller may also be operated.
Fault – CouldNotFix: Camera could not self-fix the error and needs human intervention to fix the problems.

PointingAssist: Camera is in a state supporting dedicated Telescope pointing monitoring measurements (e.g., TPoints). The specific implementation may vary from telescope-to-telescope type, e.g. for a certain particular telescope type it would mean to prepare a target (“go to target mode”) in which projecting the reflected image from a star. The camera actions depend on what type of SST pointing monitoring measurement is undertaken. It can e.g., acquire slow signal data exclusively.

11.1.2 Performance monitoring

The performance of the camera will need to be routinely characterized also during camera operation, due to aging effects of the camera components and variations in ambient conditions such as temperature or NSB. When possible, two or more independent and complementary methods of camera performance characterization will be used, to allow for cross-checking of results, estimation of systematic uncertainties, and redundancy.

The camera design includes a system to provide calibration and performance monitoring by illuminating its focal plane with fast pulses of light of variable intensity from the LED Flashers. Camera performance can also be monitored with muon rings, a sub-set of Cherenkov shower images, whose well-understood characteristics can be used as a reference. Continuous monitoring of critical calibration coefficients will take place nightly interleaved with Cherenkov events. Such calibration coefficients include:

ASIC calibration: The TARGET sampling ASICs contain a buffer of 4096 capacitive cells per pixel used to store the signal whilst a camera trigger decision is made. Each cell requires calibration. The majority of the calibration (transfer functions and temperature dependence) is required only once (at commissioning). During operation the cell 'pedestal' values, corresponding to the number of digital counts per cell with no input, will be measured at most every hour, by means of dedicated, 5-seconds long TARGET-pedestal runs.

Pixel baseline and fluctuations: The camera can periodically force a trigger, generating "pedestal" events whose data can be used to establish the baseline values and fluctuations of each pixel waveform readout. Alternatively, baselines can be determined from blank regions of shower images, or from samples preceding the trigger in the waveforms. Another use of the forced triggers is to determine the electronics baseline noise (i.e., independent of NSB or SiPM dark-count contribution) in zero bias conditions, which is accomplished by taking data while the SiPM Bias Voltage is off.

Pixel On-line Amplitude Matching & Monitoring: During normal observations, temperature and NSB level affect the SiPM gains, which will be monitored using the internal illumination system by interleaving medium-brightness flashes (e.g., 200 photons) to normal Cherenkov triggers (at ~10 Hz). Following a drift in response exceeding some threshold (~10%) the gain can be adjusted by changing the SiPM Bias Voltage. The amplitude of recorded pulses may also drift on longer timescales due to changes in the camera window transmission. To correct for such effects, a monthly 5 minutes long run using the under-window illumination system will be performed to re-establish nominal bias voltage values. This measurement requires stable light pulse intensity over long time.

Pixel Off-line Amplitude Matching (Intensity Flat Fielding): When calibrating the data, a relative correction factor called flat-field coefficient is applied to the extracted charge of each pixel to account for any differences remaining after amplitude-matching. Flat-field coefficients can be obtained by illuminating the camera with medium-brightness pulses and deconvolving the known illumination pattern. In this case the absolute brightness of the illuminating LED is not important. The flat-field coefficients include relative differences in PDE, OCT and gain between pixels. If the absolute illumination level of the LED is known and stable this measurement can also be used to determine the absolute conversion of measured charge to photoelectrons.

Pixel Off-line Time Matching (Time Flat Fielding): If the camera illumination is uniform and synchronous, the skew between the pulses recorded in the camera waveforms and trigger patterns can be used to correct for systematic pixel timing offsets. Correction offsets can be extracted from this data in a similar way as for the flat-field coefficients. See Appendix A2 for further details.

Broken / Malfunctioning Pixels: Pixels can be easily identified as broken or malfunctioning continuously during normal data taking via the aforementioned interleaved flasher pulses.

Pixel linearity: The calibration measurements mentioned so far utilise a medium-illumination level. The performance as a function of illumination level (<1 to >1000 p.e.) will be monitored during operation via the LED flashers in dedicated runs expected to take place weekly.

Single-photo electron response: The LED flashers units are capable of illuminating the camera at the single p.e. level. The mean relative illumination level as compared to that expected gives an indication of the degradation to the combination of M2 reflectivity, camera entrance window transmission, SiPM PDE (assuming a stable LED brightness). The variation between pixels in extracted illumination level indicates the relative PDE of each pixel (assuming this dominates over non-uniformity of the illumination pattern – specified to be 2% over the camera). Due to the high number of events (10 – 20 k) needed to produce a well resolved single p.e. spectrum it is unlikely that low-illumination flashes are interleaved with normal data taking. Therefore, dedicated runs of ~80 s are expected nightly. It should be noted that gain and optical cross talk may also be established independently of the LED flashers via dark counts. The use of this in routine monitoring is yet to be established.

Total Optical Throughput Efficiency: Reliable calibration and monitoring of the telescope optical throughput efficiency is required to convert the recorded image intensity from p.e. to photons. The total throughput is a combination of: mirror reflectivity, shadowing, camera window transmission and SiPM PDE and can be extracted from the ring–like images generated by background muons. Ring-like images are fitted to extract geometrical parameters which can then be used to calculate the amount of light emitted by a muon. Comparing the extracted image size in p.e. to the theoretical expectation for the same ring geometry enables the telescope–wise optical throughput efficiency to be determined. Events containing muon rings will therefore be flagged by the camera and their data saved. For an event to be a muon candidate, it must pass the normal Camera Unit trigger scheme. At the event-builder software, events are then held whilst the array-level trigger looks for coincidences between telescopes and sends a request for the data to be retained. In addition to this, each Camera event builder may retain a certain fraction of events as muon candidates. To identify candidates, the software examines the L0 trigger pattern events in real time with a technique described in [RD14]. An efficient muon tagging trigger can be implemented by simply counting L0 trigger patches (superpixels) as shown in Figure 90.

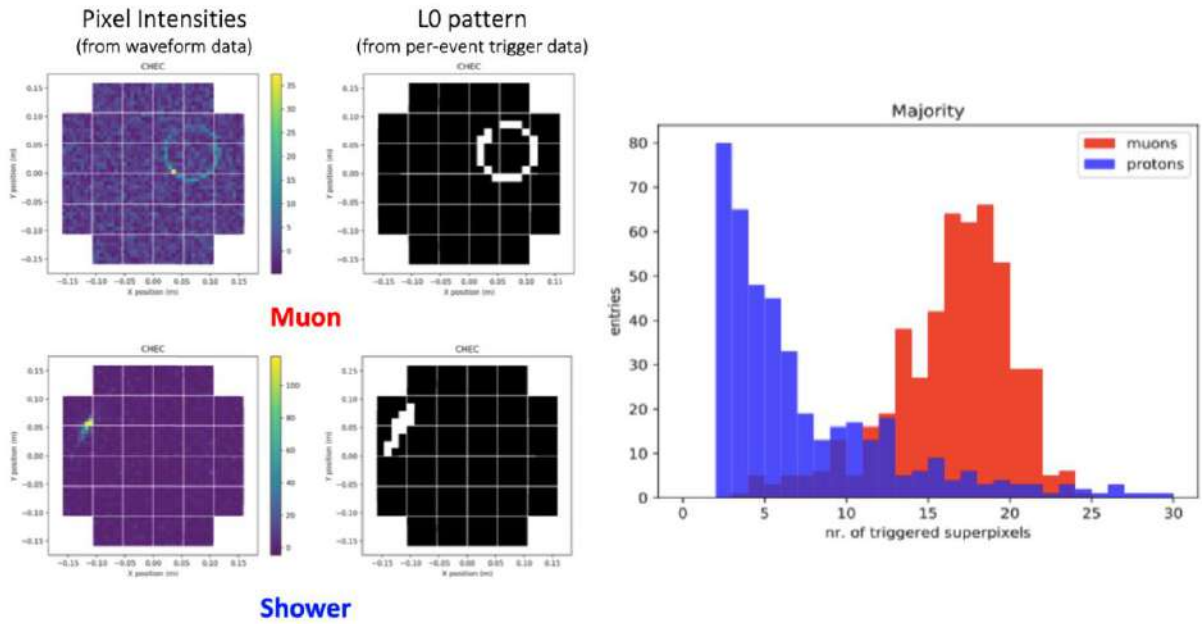


Figure 90: Left: Simulated muon and shower image, as represented both by the extracted charge from waveforms, and by the L0 (superpixel) pattern. Right: Distributions of L0 hits for muons and protons, showing that a cut on the number of superpixels in a given event can be used to identify muon candidates.

11.1.3 Typical Operation Monthly Cycle

- The SST Camera spends the daylight hours in the **Initialized** state.
- Roughly one hour before the beginning of the observations, the command warmUp is issued. Warming up takes about 40 minutes.
- Upon entering the **Standby – Idle** state, the SST Camera is configured by the command configureCamera which has it reach the **Ready – Idle** state, which is immediately followed by an internal calibrate command, bringing the camera in its **Ready – Calibrating** state.
- In this state, the camera starts a 5 seconds ASIC calibration run (see Section 11.1.2). After this, baseline zero-bias calibration runs and single p.e. runs are taken. A pixel linearity run per week is taken during the waning moon phase, after the end of astronomical twilight. The camera then returns into the **Ready – Idle** state via the internal calComplete command.
- When receiving a startObserving command, the camera starts an observation run in the **Observing** mode.
- The run is stopped by the goToReady command, which brings the camera back to **Ready – Idle.**
- Another 5 seconds ASIC calibration run is taken via the **Ready – Calibrating** state if more than an hour has elapsed, or the camera temperature has changed by a significant amount.
- The camera goes back to **Observing** as requested, and the cycle is repeated throughout the night.
- At the end of the night, a single p.e. and zero-bias calibration runs are taken in the **Ready – Calibrating** state. A pixel linearity run per week is taken during the waxing moon phase, before the beginning of astronomical twilight. During the waxing gibbous moon week, a pixel amplitude matching run is also taken.

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